■ MB81416-10, MB81416-12, MB81416-15

NMOS 65,536-Bit Dynamic Random Access Memory

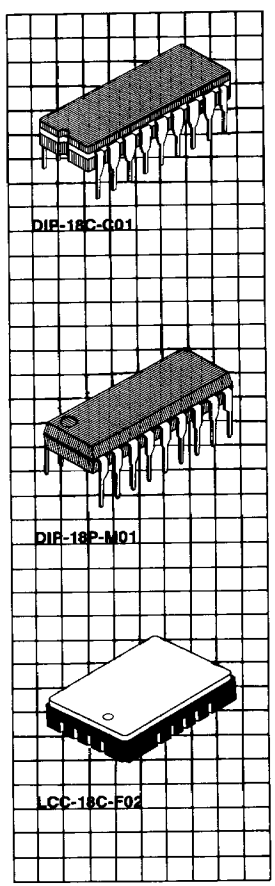
Description

The Fujitsu MB81416 is a fully decoded, dynamic NMOS random access memory organized as 16384 words by 4-bits. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB81416 to be housed in a standard 18-pin DIP that is compatible with the JEDEC approved pinout. Greater refresh versatility is provided by a new $\overline{CAS}$ before $\overline{RAS}$ on-chip refresh capability. The MB81416 also features "page mode" which allows high speed random access of up to 64 nibble wide words within the same row address.

The MB81416 is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and the power supply tolerance is very wide. All inputs and outputs are TTL compatible.

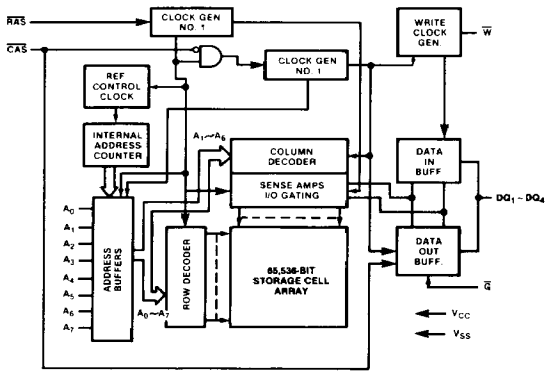


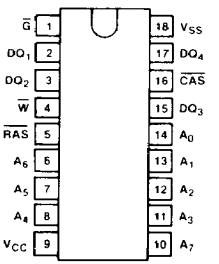
Features

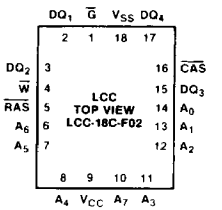
- Organized as 16384 words by 4-bits
- Row Access Time/Cycle Time:
  MB81416-10 100nsec max/200 min.
  MB81416-12 120nsec max/230 min.
  MB81416-15 150nsec max/260 min.
- Low Active Power (t_{RC} = min)
  MB81416-10 303mW (max.)
  MB81416-12 275mW (max.)
  MB81416-15 248mW (max.)
  All devices 25mW standby
- Single +5V ±10% Power Supply
- $\overline{CAS}$ before $\overline{RAS}$ Refresh
- $\overline{RAS}$ Only Refresh
- Hidden $\overline{CAS}$ before $\overline{RAS}$ Refresh
- 2ms/128 cycle Refresh (A_0~A_6)
- Read-Modify-Write Capability
- Page Mode Capability for faster access
- Output unlatched at cycle end
- Early Write or Output Enable controls output buffer impedance
- On Chip Address and Data-In latches
- Standard 18-pin DIP
- All Inputs TTL Compatible, low capacitive load
- Three-State TTL Compatible Outputs
- On-chip Substrate Bias Generator

NOTE: The following IEEE Std. 662-1980 Symbols are used in this data sheet: DQ = Data I/O, $\overline{G}$ = Output Enable and $\overline{W}$ = Write Enable.

MB81416 Block Diagram and Pin Configurations







Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance
($T_A = 25°C$)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_7$,	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{G}$	C_{IN2}	—	8	pF
Output Capacitance $DQ_1 \sim DQ_4$	C_D	—	7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs except DQ	V_{IL}	−2.0	—	0.8	V	
Input Low Voltage, DQ	V_{ILD}*	−1.0	—	0.8	V	

*The device will withstand undershoots to the −2.0V level with a maximum pulse width the 20ns at the −1.5V level.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT*	MB81416-10			55	
Average power supply current	MB81416-12	I_{CC1}		50	mA
($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB81416-15			45	
STANDBY CURRENT		I_{CC2}		4.5	mA
Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})					
REFRESH CURRENT1*	MB81416-10			38	
Average power supply current	MB81416-12	I_{CC3}		35	mA
($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB81416-15			32	
PAGE MODE CURRENT	MB81416-10			38	
Average power supply current	MB81416-12	I_{CC4}		35	mA
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min)	MB81416-15			32	
REFRESH CURRENT 2*	MB81416-10			42	
Average power supply current	MB81416-12	I_{CC5}		38	mA
($\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$)	MB81416-15			35	
INPUT LEAKAGE CURRENT					
Input leakage current, any input					
($0 \leq V_{IN} \leq 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$,		I_{IL}	−10	10	μA
all other pins not under test = 0V)					
OUTPUT LEAKAGE CURRENT		I_{OL}	−10	10	μA
(Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)					
OUTPUT LEVELS					
Output high voltage (I_{OH} = −5mA)		V_{OH}	2.4		
Output low voltage (I_{OL} = 4.2mA)		V_{OL}		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is dependent on input low voltage level V_{ILD}, $V_{ILD} > -0.5V$.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

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Parameter	Notes	Symbol Alternate	*Standard	MB81416-10 Min	MB81416-10 Max	MB81416-12 Min	MB81416-12 Max	MB81416-15 Min	MB81416-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV	—	2	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	290	—	330	—	375	—	ns
Access Time from $\overline{RAS}$	(4), (6)	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$	(5), (6)	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn Off Delay		t_{OFF}	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	50	—	60	—	75	—	ns
$\overline{CAS}$ Precharge Time (Page Mode only)		t_{CP}	TCEHCEL	45	—	50	—	60	—	ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	TCEHCEL	40	—	45	—	55	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	100	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	(4), (7)	t_{RCD}	TRELCEL	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEHREL	20	—	25	—	30	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	(9)	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Read Command Hold Time Referenced to $\overline{CAS}$	(9)	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Write Command Set Up Time		t_{WCS}	TWLCEL	−5	—	−5	—	−5	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	20	—	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	20	—	25	—	30	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	45	—	50	—	60	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	45	—	50	—	60	—	ns
Data In Set Up Time		t_{DS}	TDVCEL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	20	—	25	—	30	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay	(8)	t_{CWD}	TCELWL	85	—	100	—	120	—	ns
$\overline{RAS}$ to $\overline{W}$ Delay	(8)	t_{RWD}	TRELWL	135	—	160	—	195	—	ns
Access Time from $\overline{G}$		t_{OEA}	TGLQV	—	25	—	30	—	40	ns
$\overline{G}$ to Data in Delay Time		t_{OED}	TGHDV	30	—	35	—	40	—	ns
$\overline{G}$ Hold Time Referenced to $\overline{W}$		t_{OEH}	TWLGL	0	—	0	—	0	—	ns
Output Buffer Turn Off Delay from $\overline{G}$		t_{OEZ}	TGHQZ	0	30	0	35	0	40	ns
Page Mode Cycle Time		t_{PC}	TCELCEL	105	—	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	180	—	205	—	240	—	ns
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{FCS}	TCELREL	20	—	25	—	30	—	ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{FCH}	TRELCEH	20	—	25	—	30	—	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20	—	20	—	20	—	ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	(10)	t_{TRAS}	TRELREH	280	—	325	—	390	—	ns
Refresh Counter Test Cycle Time	(10)	t_{RTC}	TRELREL	380	—	435	—	500	—	ns
$\overline{G}$ to $\overline{RAS}$ Inactive Setup Time		t_{OES}	TGLREH	0	—	0	—	0	—	ns
Data in to $\overline{CAS}$ Delay Time	(11)	t_{DZC}	TDXCEL	0	—	0	—	0	—	ns
Data in to $\overline{G}$ Delay Time	(11)	t_{DZO}	TDXGL	0	—	0	—	0	—	ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ cycle)		t_{CPR}	TCEHCEL	25	—	30	—	30	—	ns

Notes: See notes on next page.

*These symbols are described in IEEE Std. 662-1980: IEEE Standard Terminology for Semiconductor Memory.

AC Characteristics
(Continued)

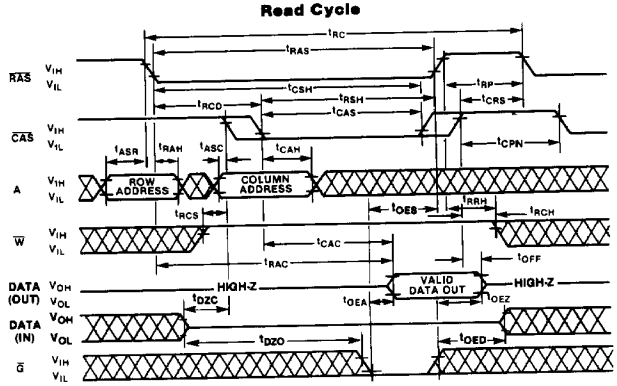
Notes:

1. An initial pause of 200μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T = 5ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.): t_T = 5ns.
8. t_{WCS}, t_{CWD} and t_{RWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.

   If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Refresh counter test cycle only.
11. Either t_{DZC} or t_{DZO} must be satisfied for all cycles.

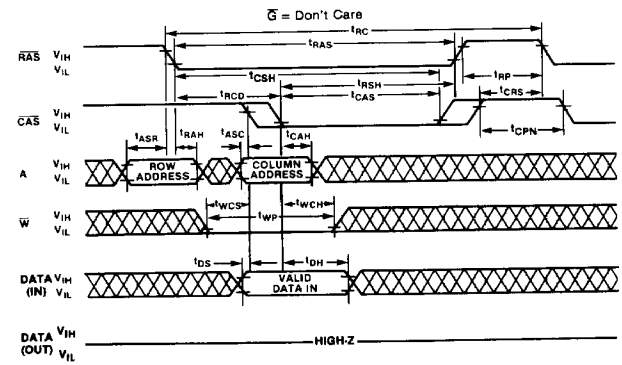
Timing Diagrams

Read Cycle



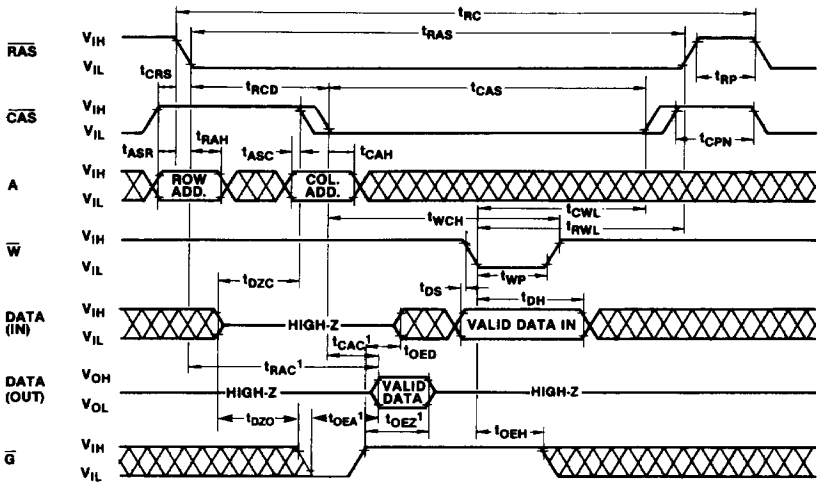
Write Cycle (Early Write)

$\overline{G}$ = Don't Care



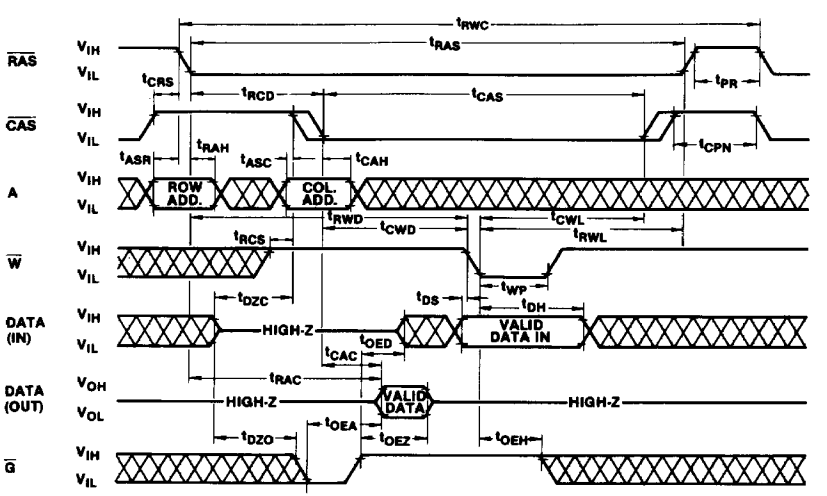
Timing Diagrams
(Continued)

Write Cycle
(Output Enable Controlled)



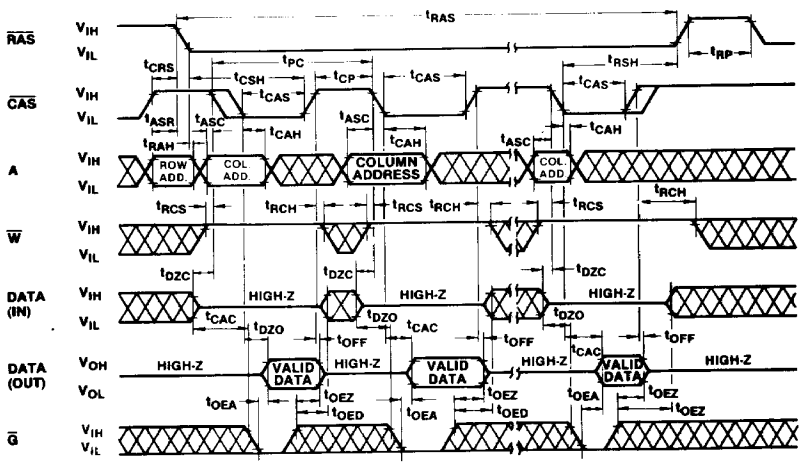
Note 1: When t_{CWD} is satisfied and $\overline{G}$ is low (Delayed-Write Cycle), the data out will be "VALID". But when t_{CWD} is not satisfied, the data out will be "INVALID".

Read-Write/Read-Modify-Write Cycle



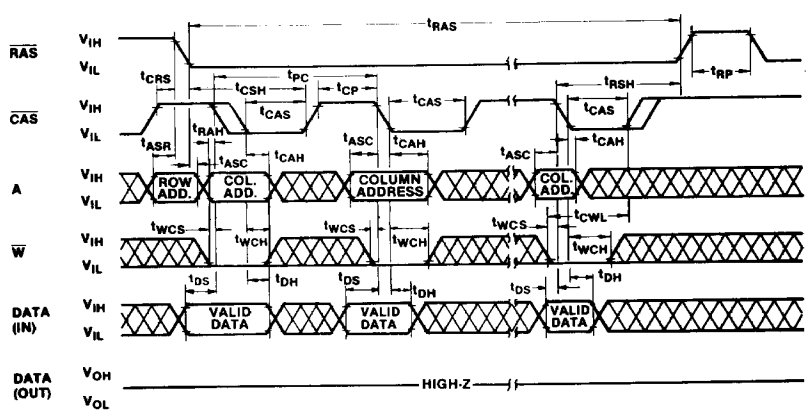
Timing Diagrams
(Continued)

Page Mode Read Cycle



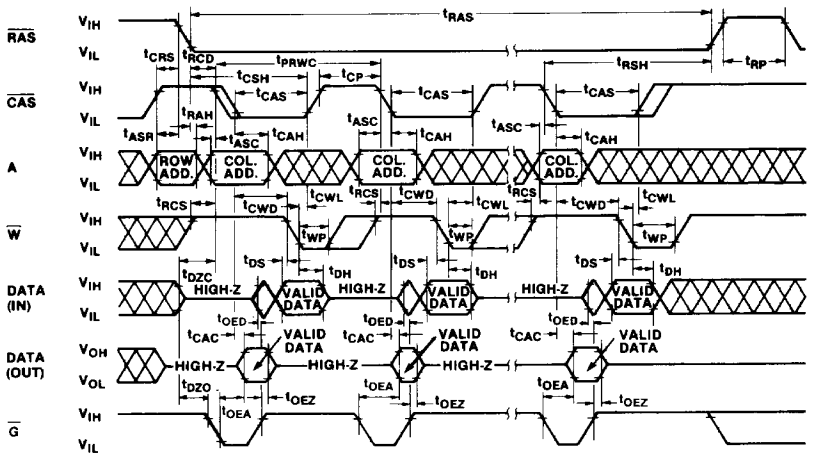
Page Mode Write Cycle

(G = Don't Care)

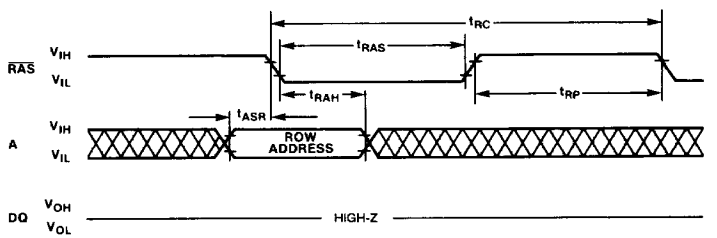


Timing Diagrams
(Continued)

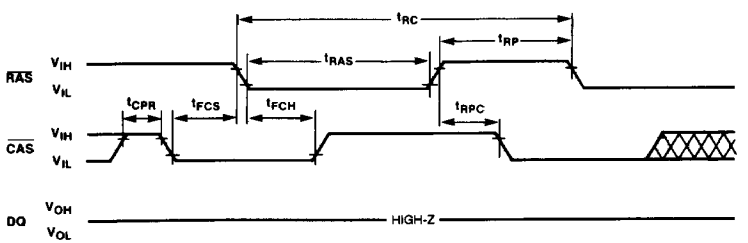
Page Mode Read-Write Cycle



RAS Only Refresh Cycle
NOTE: $\overline{CAS}$ = V_{IH}: A_7, $\overline{W}$, $\overline{G}$ = Don't Care



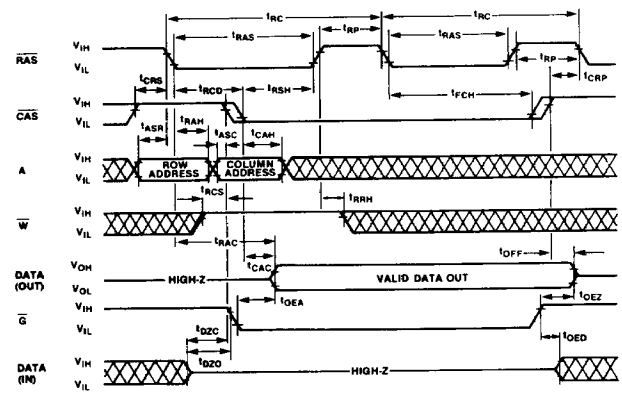
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle
NOTE: A, $\overline{W}$, $\overline{G}$ = Don't Care



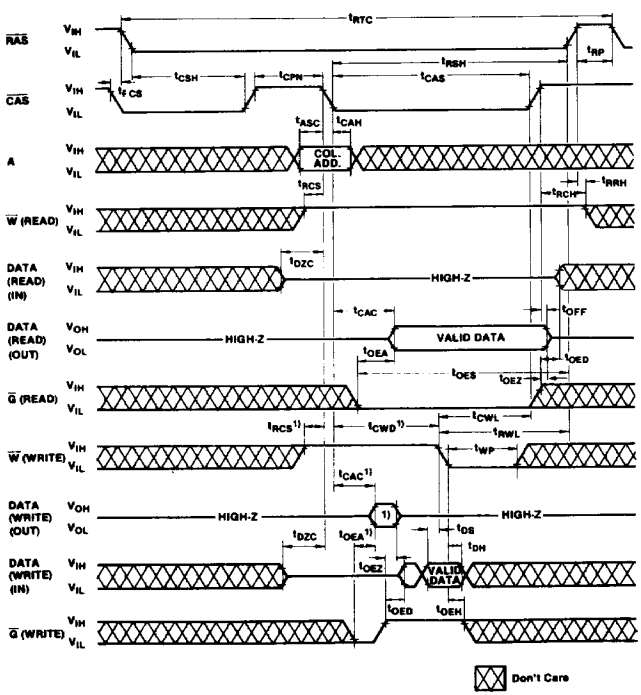
Don't Care

Timing Diagrams
(Continued)

Hidden Refresh Cycle



CAS-Before-RAS Refresh Counter Test Cycle



Note 1: When t_{CWD} is satisfied and $\overline{G}$ is Low (Delayed-Write Cycle), the data out will be "VALID". But when t_{CWD} is not satisfied, the data out will be "INVALID".

Description

Address Inputs

A total of 14 binary input address bits are needed to decode any one of 16,384 nibble wide words from the MB81416's 65,536 memory cells. Addressing a Random 4-bit word is initiated by establishing 8 row address bits on the address input pins, (A_0 through A_7), and after they are stable, latching these address bits with the falling edge of the Row Address Strobe ($\overline{RAS}$). Then 6 column address bits are established on the address input pins A_1 through A_6. After the addresses are stable, they are latched with the falling edge of the Column Address Strobe ($\overline{CAS}$). Address timing is made non-critical by the MB81416's "gated $\overline{CAS}$" circuitry which automatically inhibits $\overline{CAS}$ until the Row Address Hold time (t_{RAH}) has been satisfied and the address inputs have changed from row to column addresses.

Data Input/Output

The MB81416 has 4 common I/O pins (DQ_1, DQ_2, DQ_3, and DQ_4). Read or write modes are selected with the write enable pin ($\overline{W}$). An output enable pin ($\overline{G}$) controls the state of the output buffers making delayed write and read-modify-write cycles possible. The DQ pins provide TTL compatible inputs and three-state TTL compatible outputs with a fan-out of two standard TTL loads. Data-out has the same polarity as data-in.

Write Enable

The read mode or write modes are determined by the state of the write enable pin ($\overline{W}$). A logic high on $\overline{W}$ selects the read mode and a logic low on $\overline{W}$ selects the write mode. When $\overline{W}$ is high (read mode), the data inputs are disabled. If $\overline{W}$ goes low and satisfies the write command set-up time (t_{WCS}) before $\overline{CAS}$ goes low, the data outputs will remain in the high-impedance state for the duration of the cycle. This allows a write cycle to occur regardless of the state of the output enable ($\overline{G}$).

Output Enable

The output buffers are controlled by both $\overline{CAS}$ and output enable ($\overline{G}$). If either $\overline{CAS}$ or $\overline{G}$ are high the output buffers are in the high impedance state. During a read or read-modify-write cycle if both $\overline{CAS}$ and $\overline{G}$ are low, the output buffers are enabled. During an early write cycle $\overline{G}$ has no effect on the output buffers.

Data Inputs

Data may be written into the MB81416 during a write or read-modify-write cycle. The last falling edge of $\overline{CAS}$ or $\overline{W}$, strobes the data into the 4 on-chip data latches. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with both the set-up time (t_{DS}) and hold time (t_{DH}) referenced to the falling edge of $\overline{CAS}$. The outputs are in the high impedance state regardless of $\overline{G}$'s state. In a delayed write or a read-modify-write cycle, $\overline{W}$ is brought low after $\overline{CAS}$, data is strobed-in by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$. To avoid buss contention on I/O pins, it is necessary during a delayed write or a read-modify-write cycle for $\overline{G}$ to be high prior to data input so that the output buffers are in the high impedance state when data is being written.

Data Outputs

Data can be read from the MB81416 with either a read or a read-modify-write cycle. These cycles begin with the outputs in the high impedance state. The outputs contain active, valid data only after both $\overline{CAS}$ and $\overline{G}$ have been brought low and have satisfied the minimum access time from $\overline{RAS}$ (t_{RAC}) and the minimum access time from the output enable t_{OED}. Outputs contain valid data as long as both $\overline{CAS}$ and $\overline{G}$ are held low. They return to the high impedance state when either $\overline{CAS}$ or $\overline{G}$ go high.

$\overline{RAS}$-Only Refresh

The MB81416's dynamic memory cells may be refreshed by performing any memory cycle at each of the 128 row addresses (A_0 through A_6) at least every 2 milliseconds. When a row is accessed all bits in the row are refreshed. During refresh, A_7 (Pin 10) is not used and either V_{IH} or V_{IL} may be applied to this pin.

$\overline{RAS}$-only Refresh is a simplified cycle that consists of strobing a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. During a $\overline{RAS}$-only Refresh cycle, $\overline{CAS}$ is high and the output buffers are in the high impedance state. Strobing each of the 128 row addresses (A_0 through A_6) with $\overline{RAS}$ will refresh all 65,536 memory cells in the MB81416. $\overline{RAS}$-only Refresh results in a substantial reduction in power dissipation compared to a full $\overline{RAS}$/$\overline{CAS}$ memory cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh*

$\overline{CAS}$ before $\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set-up time (t_{FCS}) before $\overline{RAS}$ goes low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden $\overline{CAS}$ Before $\overline{RAS}$ Refresh

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$ before $\overline{RAS}$ refresh capability.

*Note: $\overline{CAS}$ Before $\overline{RAS}$ refresh available on request.

Description,
(Continued)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle provides a convenient way to verify the functionality of the $\overline{CAS}$ before $\overline{RAS}$ refresh circuitry. The cycle begins with a $\overline{CAS}$ before $\overline{RAS}$ operation. Then $\overline{CAS}$ is cycled "high" and then "low". This enables a read, write, or read-modify-write operation to occur. Four memory cells are accessed with the location defined as follows:

Row Address —
Bits A_0 through A_6 are supplied by the on-chip refresh counter. Bit A_7 is set low internally.

Column Address —
Bits A_1 through A_6 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Procedure

The $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle timing is used in each of the following steps:

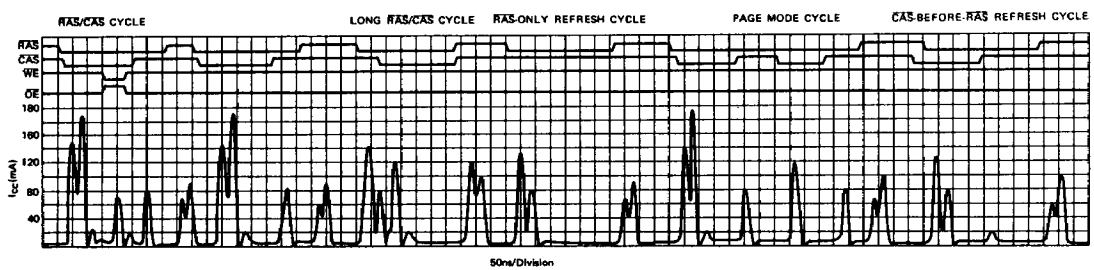
1. Initialized the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into each set of 4 memory cells at a single column address and 128 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 128 times so that "highs" are written into the 128 sets of 4 memory cells.
4. Read the highs written during step 3.
5. Compliment the test pattern and repeat steps 2, 3, and 4.

Page Mode

Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to read, write, or read-modify-write. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to setup and strobe sequential row addresses for the same page. Up to 64 nibble wide words may be accessed with the same row address.

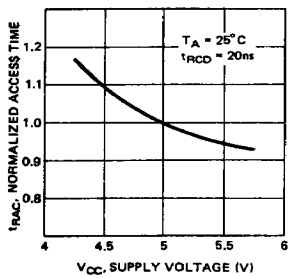
Typical Characteristics Curves

CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

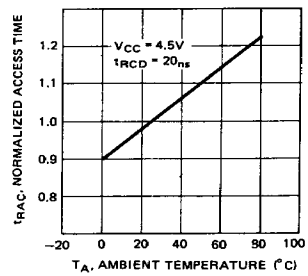


Typical Characteristics Curves
(Continued)

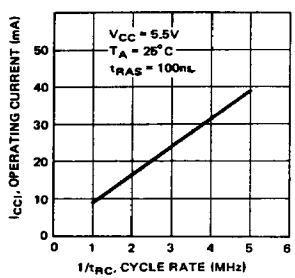
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



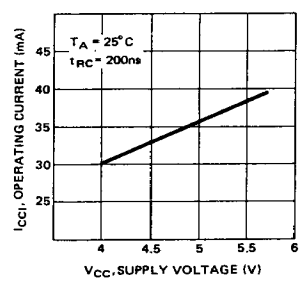
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



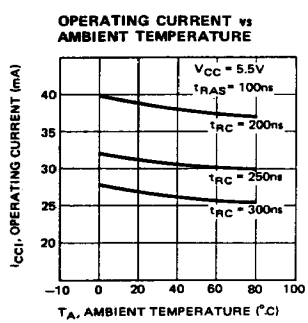
OPERATING CURRENT vs CYCLE RATE



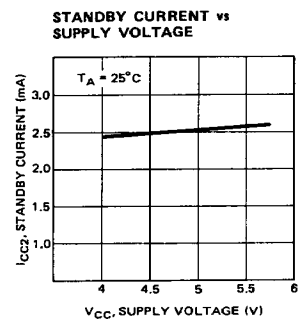
OPERATING CURRENT vs SUPPLY VOLTAGE



OPERATING CURRENT vs AMBIENT TEMPERATURE

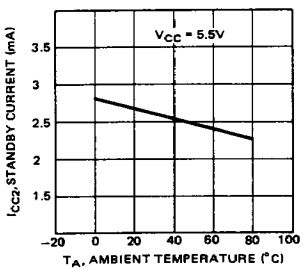


STANDBY CURRENT vs SUPPLY VOLTAGE

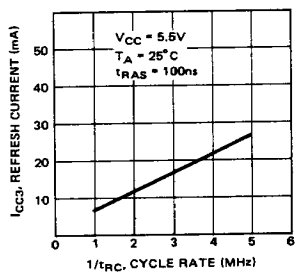


Typical Characteristics Curves
(Continued)

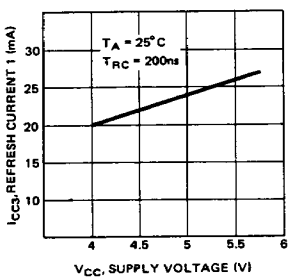
STANDBY CURRENT vs AMBIENT TEMPERATURE



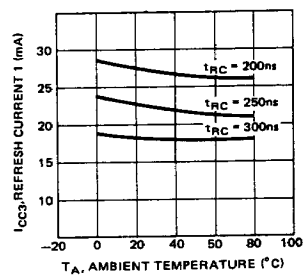
REFRESH CURRENT 1 vs CYCLE RATE



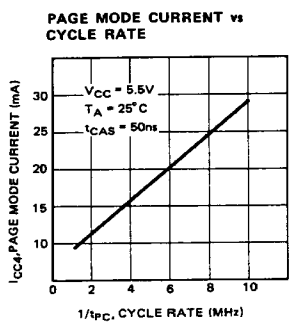
REFRESH CURRENT 1 vs SUPPLY VOLTAGE



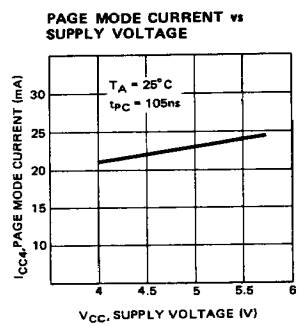
REFRESH CURRENT 1 vs AMBIENT TEMPERATURE



PAGE MODE CURRENT vs CYCLE RATE

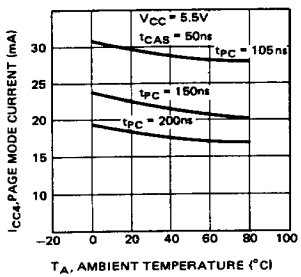


PAGE MODE CURRENT vs SUPPLY VOLTAGE

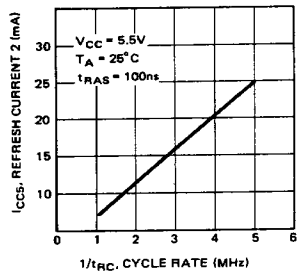


Typical Characteristics Curves
(Continued)

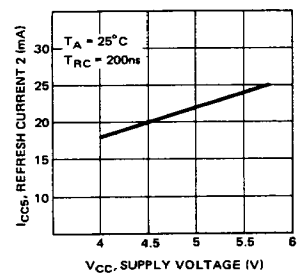
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



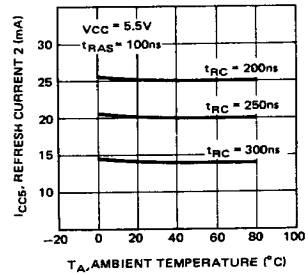
REFRESH CURRENT 2 vs CYCLE RATE



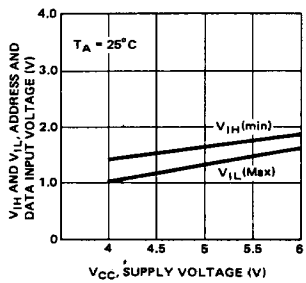
REFRESH CURRENT 2 vs SUPPLY VOLTAGE



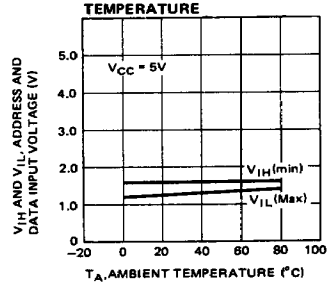
REFRESH CURRENT 2 vs AMBIENT TEMPERATURE



ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

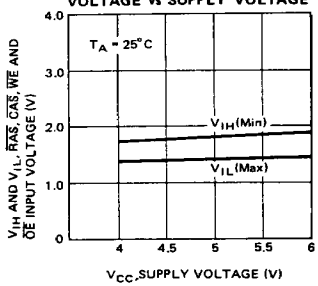


ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

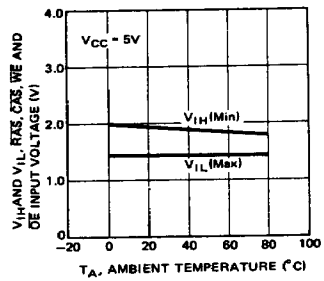


Typical Characteristics Curves
(Continued)

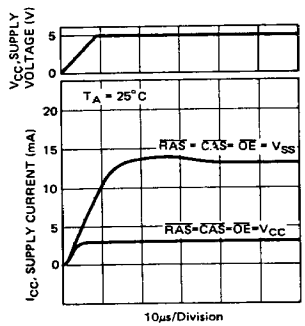
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

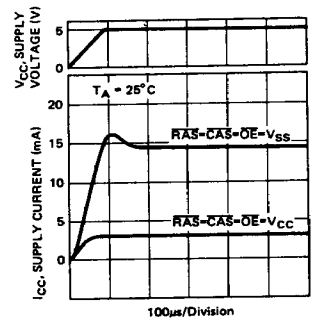


$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs AMBIENT TEMPERATURE



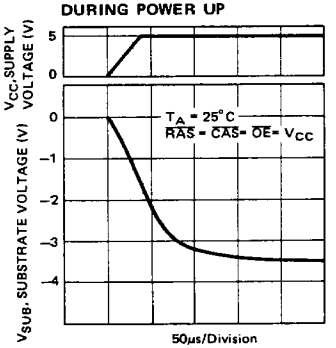
SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP



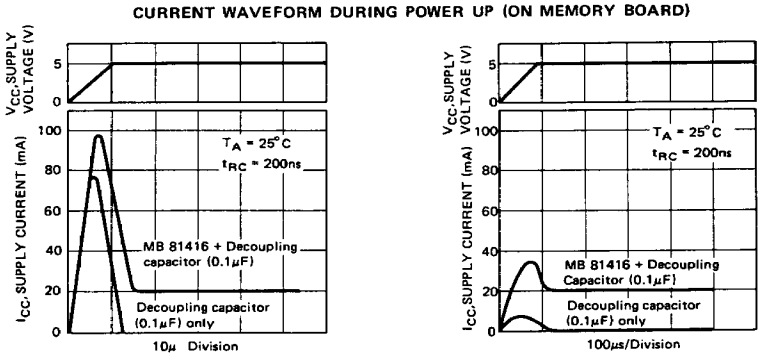


Typical Characteristics Curves
(Continued)

SUBSTARATE VOLTAGE
vs SUPPLY VOLTAGE
DURING POWER UP

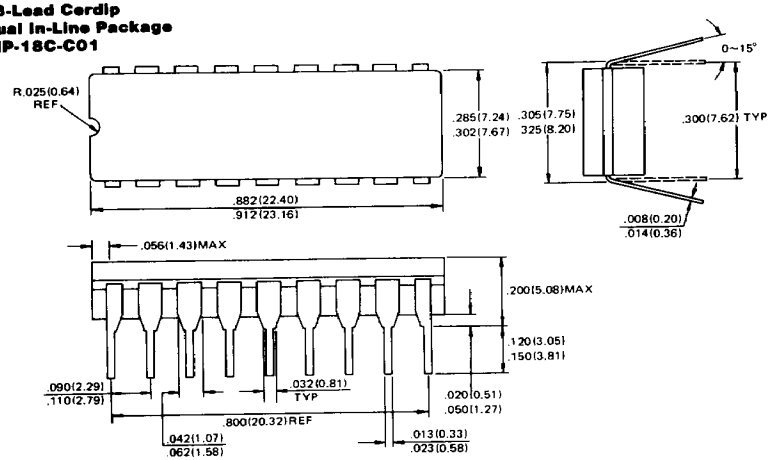


CURRENT WAVEFORM DURING POWER UP (ON MEMORY BOARD)

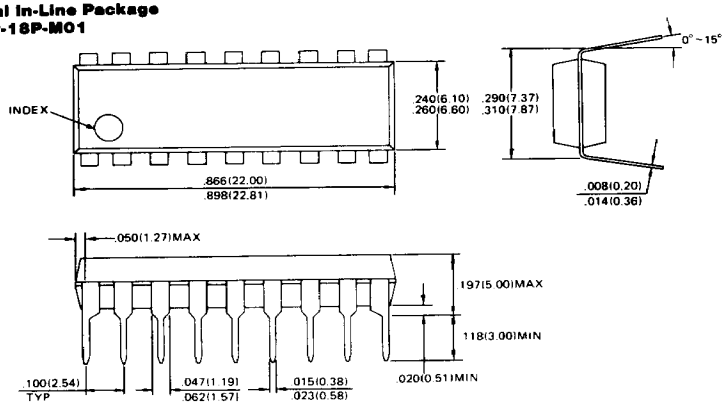


Package Dimensions
Dimensions in inches
(millimeters)

18-Lead Cerdip
Dual In-Line Package
DIP-18C-C01

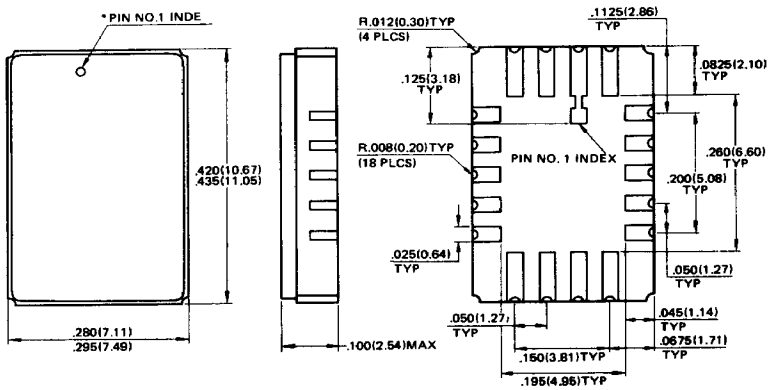


18-Lead Plastic
Dual In-Line Package
DIP-18P-M01



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F02)



*Shape of Pin 1 index: Subject to change without notice