

A-200 SERIES

(230 V Model)

MELB

TRAINING USE
ONLY

SERVICE MANUAL

Canon

SY8-0061-751

FEB. 1985

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PART I

INTRODUCTION

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I-1. General

In this section, we will give an overview to the Canon A-200 Personal Computer.

Variety of the A-200

The A-200 is classified in four versions in accordance with the types of display adapter and numbers of floppy disk drive. However, there are no single disk drive versions for 230V AC.

- Model M1..... 1 disk drive with monochrome board
- Model M2..... 2 disk drives with monochrome board
- Model C1..... 1 disk drive with color board
- Model C2..... 2 disk drives with color board

I-2. Features

• 8086 Microprocessor

The A-200 is equipped with the 8086 microprocessor as CPU (Central Processing Unit) which has 16-bit data bus. In other words, the 8086 can access 16-bit data at a time, and so, it can perform more quick and versatile data processing in comparison with an ordinary 8-bit microprocessor.

• Memories

The A-200 has 256K bytes of RAM (Random Access Memory) as the standard and is expandable up to 512K bytes. Also the A-200 is equipped with 16K bytes of system ROM (Read Only Memory) including a diagnostic program etc. and 4K bytes (Model M1 and Model M2) or 32K bytes (Model C1 and Model C2) of video RAM which stores the data to be displayed on the screen.

• Built-in Interfaces

In order to input or output data to/from the A-200, it has useful devices such as 5-1/4" floppy disk drive (Model M1 and C1 has one disk drive and Model M2 and Model C2 has two drives), RS-232C interface and printer interface.

• Expandability

In addition to the standard features listed above, a customer can expand the functions of the A-200 by adding the 8087 Numeric Data Coprocessor or inserting optional board into the internal five expansion slots.

• Powerful Operating System

A DOS (Disk Operating System) is now indispensable to the advanced personal computers like the A-200. We adopted the MS-DOS developed for 8086/8088-based computers by Microsoft Corp. Through MS-DOS, an user can communicate with the computer, disk drive, and printer, managing these resources to his advantage.

• Standard Diagnostic Programs

The A-200 has two different diagnostic programs - one is the ROM-based built-in program and the other is the disk-based programs. The ROM-based one is executed whenever the power for the computer is turned on or the RESET button is pushed. The disk-based program is an accessory of the computer. It checks the computer itself and peripherals.

• Compatible with the IBM® Personal Computer™

Most of the application software, peripherals or options designed for the IBM® PC™ can be used with the A-200.

I-3. Description of the Computer

① Power Switch

To turn the computer on or off. On-position is marked as "1" and off-position as "0". When turning on the system, turn the power of the peripherals on first then turn the computer's power switch on.

② Floppy Disk Drive(s)

To save or load programs, files or data. There are different two versions in the number of disk drives: A-200 Model M1 and C1 have only one drive and Model M2 and Model C2 have two drives.

③ RESET Button

To reset and initialize the computer when it has "hang-up" caused by improper user's program or some machine-language programs. Whenever this button is pressed, the computer will begin to execute the self diagnostic tests and then re-loads the DOS or other system disk to initialize the system.

④ Keyboard Connection Jack

To connect a coiled cable with a plug from the keyboard unit into this jack.

⑤ Keyboard

To utilize when entering commands etc.

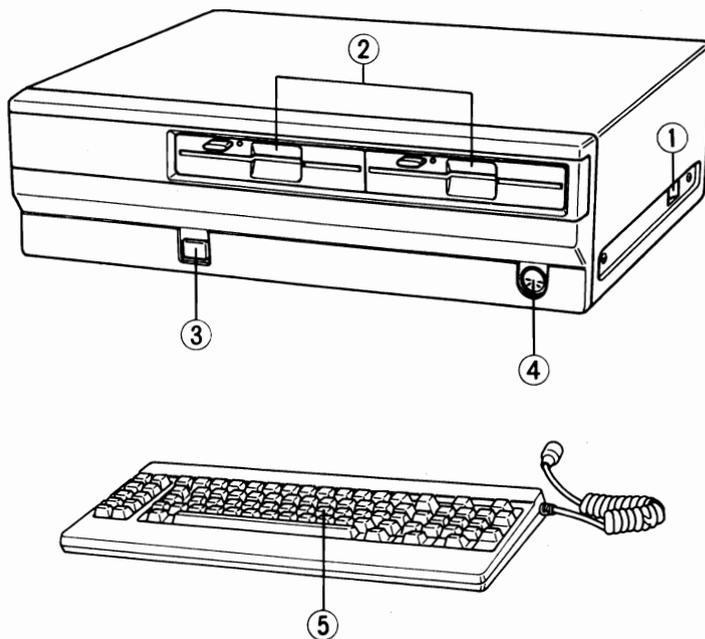


Figure 1-1

⑥ Cooling Fan

To prevent the computer against excessive heat generated during operation. Do not block this ventilation when the computer is installed close to the wall etc.

⑦ AC Power Inlet

To insert AC power cord with jack into this inlet.

⑧ AC Power Outlet

To plug a power cord of a peripherals unit etc. into this outlet. This outlet is controlled by the power switch ①. When the power switch is turned on, this outlet is powered, and when the power switch is off, this outlet is not powered.

This outlet can handle AC current in maximum of 0.4A. Be careful not to exceed this figure when using this outlet.

⑨ RS-232C Connector

To plug a special cable to this connector when an user needs to communicate with a host computer, another personal computer or serial printer.

⑩ Printer Connector

To print out data, information or programs, connect a printer cable to this connector.

⑪ Expansion I/O Slots

The Canon A-200 can expand its functions by plugging in optional expansion cards into these expansion slots.

⑫ Composite Signal Jack

This RCA-type jack has been provided for the color display adapter board only. Connect it to a composite signal input terminal on a display monitor.

⑬ Display Connector

To connect 9-pin plug with cord suitable for this connector to make a connection with the computer and the display monitor unit.

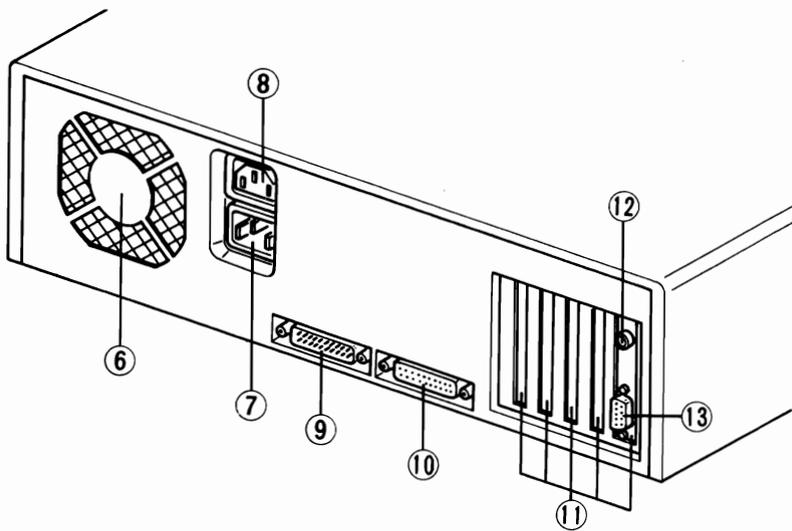


Figure 1-2

⑭ Pocket

This pocket is provided for the Model M1 and Model C1. Keep unused disks in it.

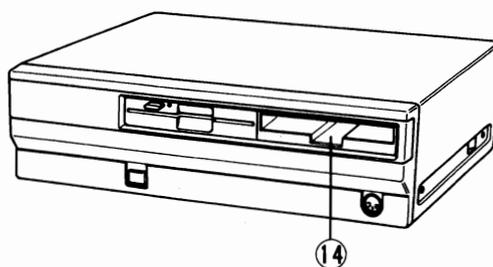


Figure 1-3

PART II

SPECIFICATIONS

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II-1. Product Outline

II-1-1. System Configuration

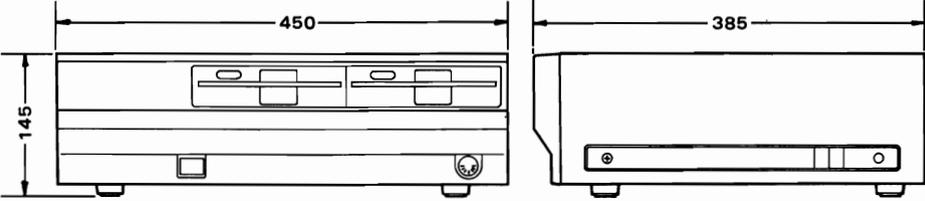
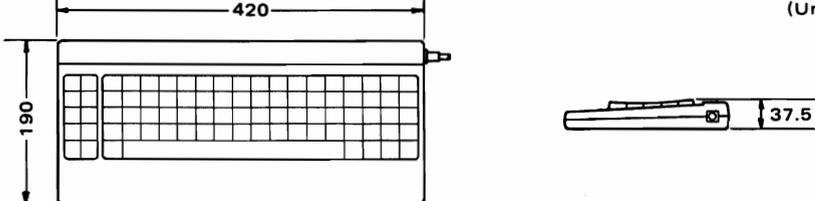
Software

OS: MS-DOS version 2.11 (Compatible with PC-DOS)

Language: GW-BASIC version 2.01

II-2. Specifications

II-2-1. General

Item	Specifications	
Size of Main Unit		
Size of Keyboard	 <p style="text-align: right;">(Unit: mm)</p>	
Weight	Approximately 11.5kg	
Power Source	230V AC $\pm 15\%$, 50/60Hz, approximately 150W	
CPU	Processor	16-bit processor 8086
	Clock	4.77MHz
	Interrupt	Eight types
Main Memory	Capacity	256K bytes (with a parity bit) + 256K EXPANSION
	Element	MOS LSI 64K bit D-RAM
FDD	Type 2-side double-density, standard track, 5-1/4" (Thin type)	
	Capacity	360K bytes/drive (Formatted)
	Format	IBM format
Serial Interface	RS-232C type, one port (on the main board) 110 — 9,600 baud programmable Connector, pin assignment IBM-PC compatible	
Printer Interface	Centronics type (on the main board) Connector, pin assignment IBM-PC compatible	
I/O Slot	Five slots 8-bit/16-bit data bus slot: Two slots (One of those used for CRT CONT.) IBM-PC compatible slot: Three slots	

II-2-2. Monochrome Display Adapter Board

Item	Specifications	
CRTC	68B45	
Video-RAM	Capacity	4K bytes
	Element	MOS LSI 16K-bit static RAM
Character Generator	Capacity	8K bytes
	Element	C-MOS masked ROM
Characters	80 characters × 25 lines 9 × 14 dots per character box 7 × 9 dots per character font Attribute IBM-PC compatible	
Video signal	16.257MHz maximum	
V-sync	50Hz	
H-sync	18.432kHz	

II-2-3. Color Display Adapter Board

Item	Specifications	
CRTC	68B45	
Video-RAM	Capacity	32K bytes
	Element	MOS LSI 64K-bit D-RAM
Character Generator	Capacity	8K bytes
	Element	C-MOS masked ROM
Characters	80 characters × 25 lines mode 8 × 8 dots per character box 7 × 7 dots per character font Attribute IBM-PC compatible; 16 colors	
	40 characters × 25 lines mode 16 × 8 dots per character box 14 × 7 dots per character font Attribute IBM-PC compatible; 16 colors	
Graphics	640 × 200 dots mode (color disable) 8 pixels per byte	
	320 × 200 dots mode (color graphics) 4 pixels per byte; one pixel can be assigned 4 of 16 colors.	
Video signal	14.31818MHz maximum	
V-sync	60Hz	
H-sync	15.75kHz	

II-2-4. Floppy Disk Drive MDD-211

Item	Specifications	
Type	2-side, double-density, standard track, 5-1/4" (Thin type)	
Weight	1.2kg	
Storage Capacity	Total	327.68K bytes (Formatted)
	Per track	6.25K bytes
Number of Tracks	80	
Number of Sectors	16	
Recording Density	5876 BPI	
Data transfer Rate	250K bits per second	
Access Time	Between tracks	6 mS
	Seek settling	20 mS
	Revolution waiting	100 mS
Error Rate	10^{-12} per bit, 10^{-6} per seek	
Power Consumption	+5V, 0.4A max., +12V, 1.0A max.	

II-2-5. Keyboard Unit

Item	Specifications
Processor	8-bit one-chip microprocessor 8048 (or 8748)
Number of Keys	83 keys
Weight	Approximately 1.6kg

- Key Layout

USA, ASCII

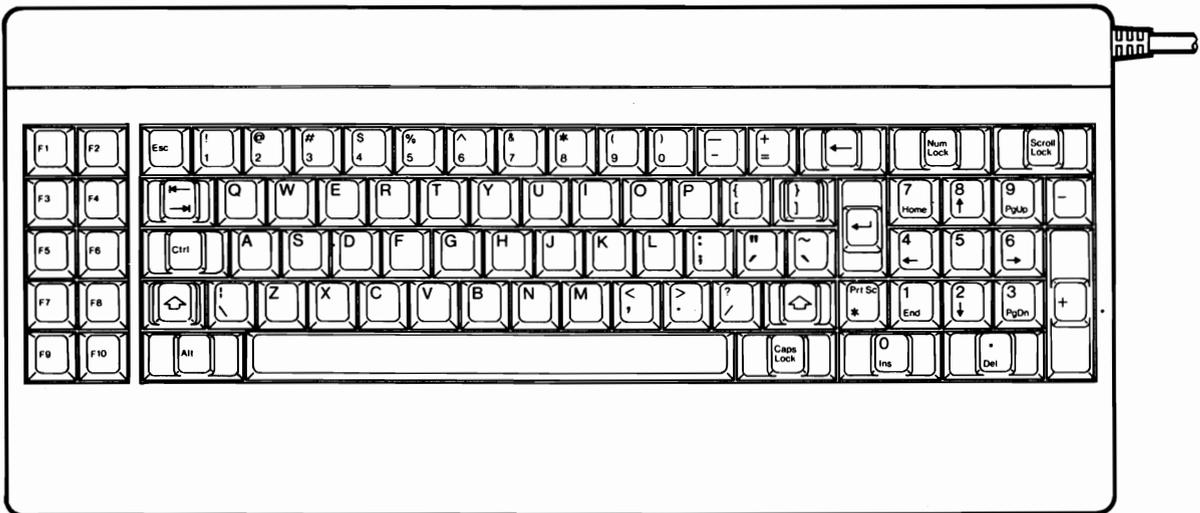


Figure 2-1

UK

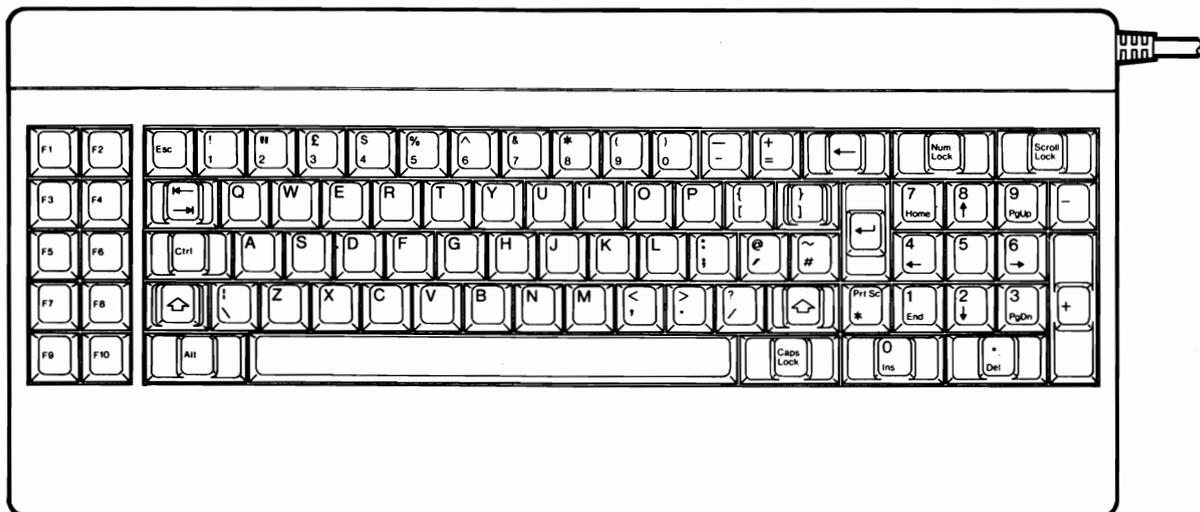


Figure 2-2

GERMAN

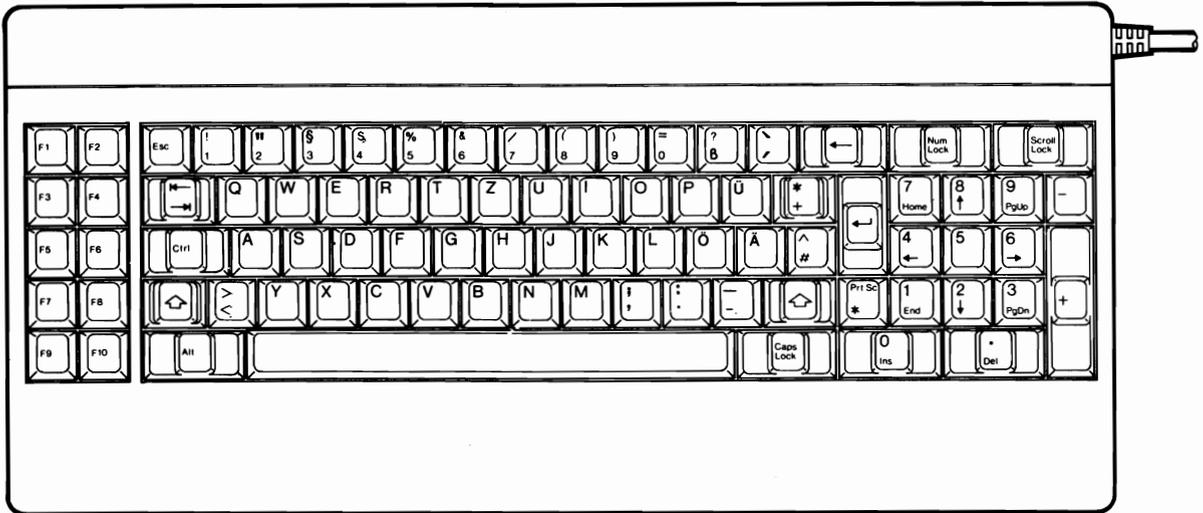


Figure 2-3

FRENCH

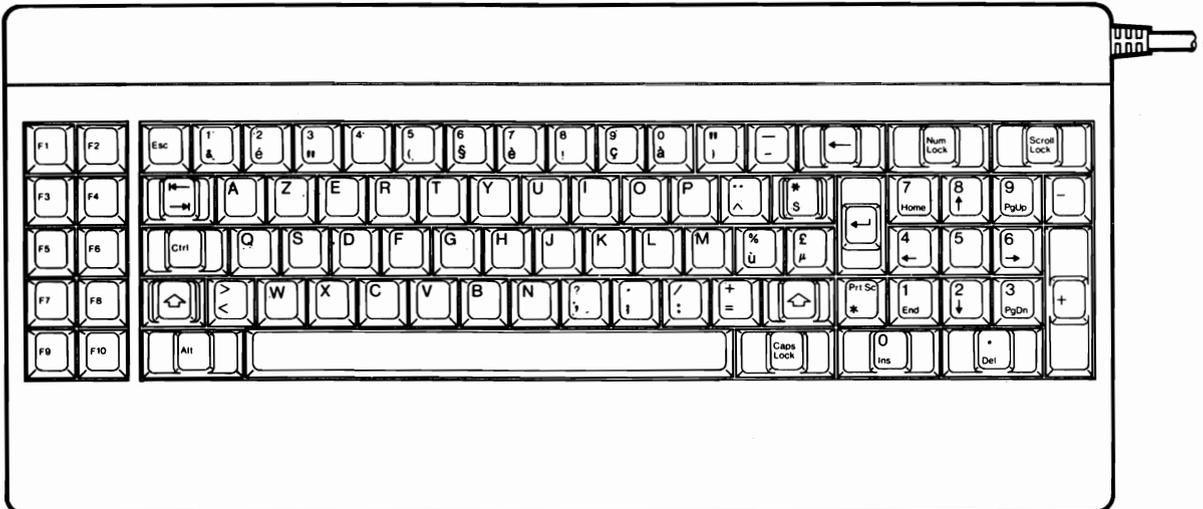


Figure 2-4

PART III

DISASSEMBLY PROCEDURE

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III-1. Disassembly Procedure

Notes

- Be sure to turn the power switch of the A-200 off and to unplug the AC cord from the outlet.
- Use screw drivers whose tip fits the head of screws or you may damage the head.

III-1-1. Top Cover

1. Remove four screws from both sides of the top cover.
2. Lift the rear of the top cover and move it backward.

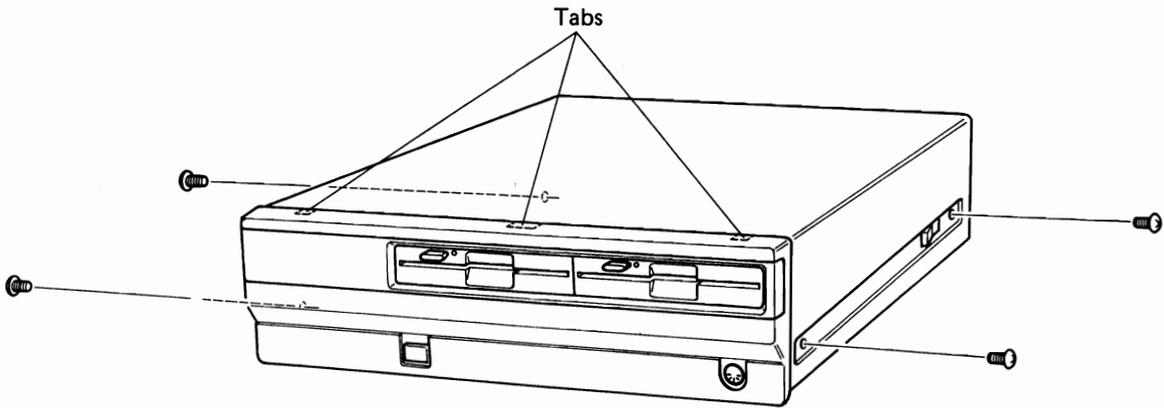


Figure 3-1

III-1-2. Power Unit

1. Unplug the AC power cords from the inlet and outlet located on the rear of the computer.

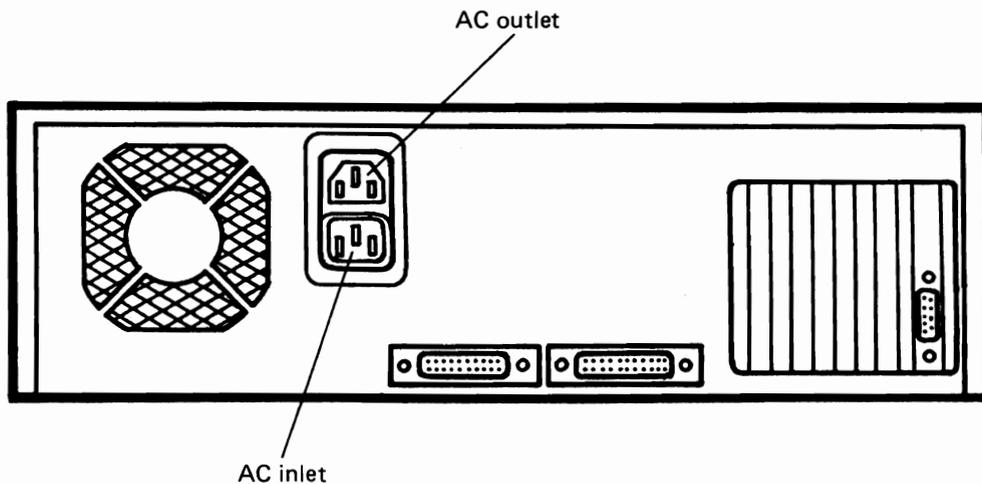


Figure 3-2

2. Disconnect the power supply cables from the floppy disk drives.

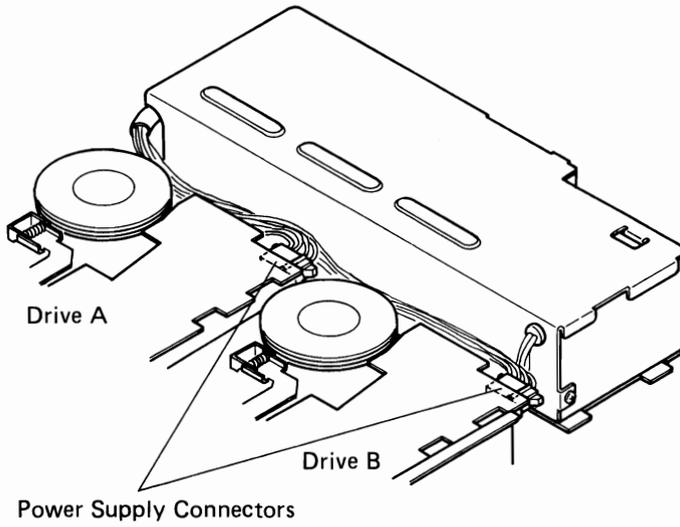


Figure 3-3

3. Disconnect the cable from the power switch. In this case, push the tab (A) on the connector and pull away the connector (B).

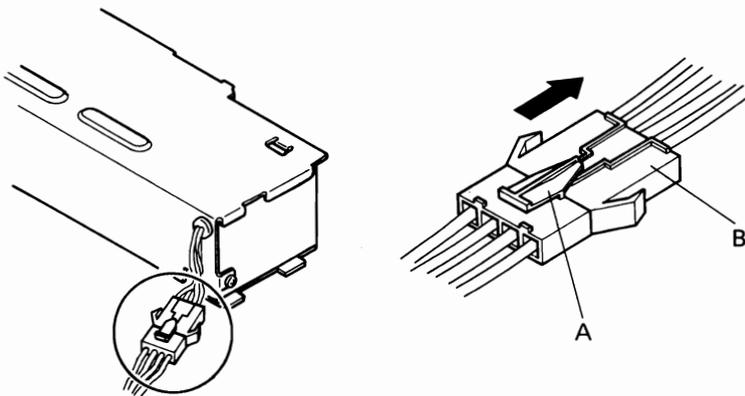


Figure 3-4

4. Loosen the screw (A) and remove the screw (B).

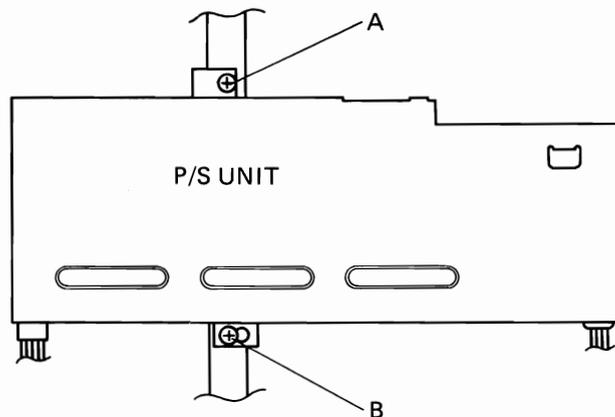


Figure 3-5

- The right side of the power unit is secured to the chassis with two tabs. Move the power unit to the left until these tabs become free from the chassis.

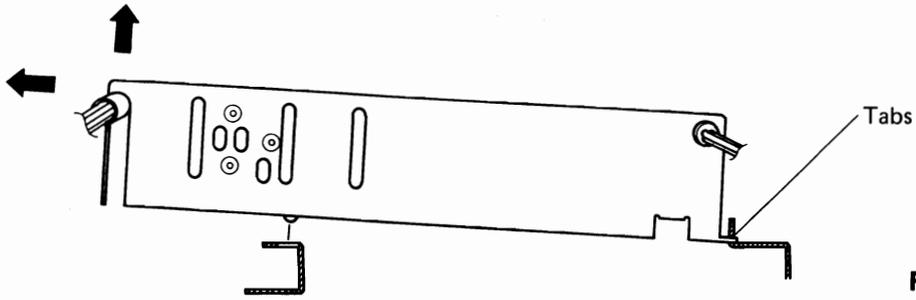


Figure 3-6

- Disconnect the cables from the main P.C.B. in the same manner as the power switch cable.

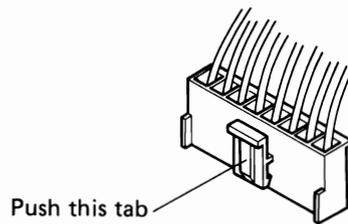


Figure 3-7

III-1-3. Main P.C.B.

- Remove the top cover.
- Remove the power unit.
- If any optional board such as display adapter or RAM board is inserted into the optional slots, remove that board.
- Remove cables from the speaker, keyboard connector, RESET switch, floppy disk drives and the cooling fan.

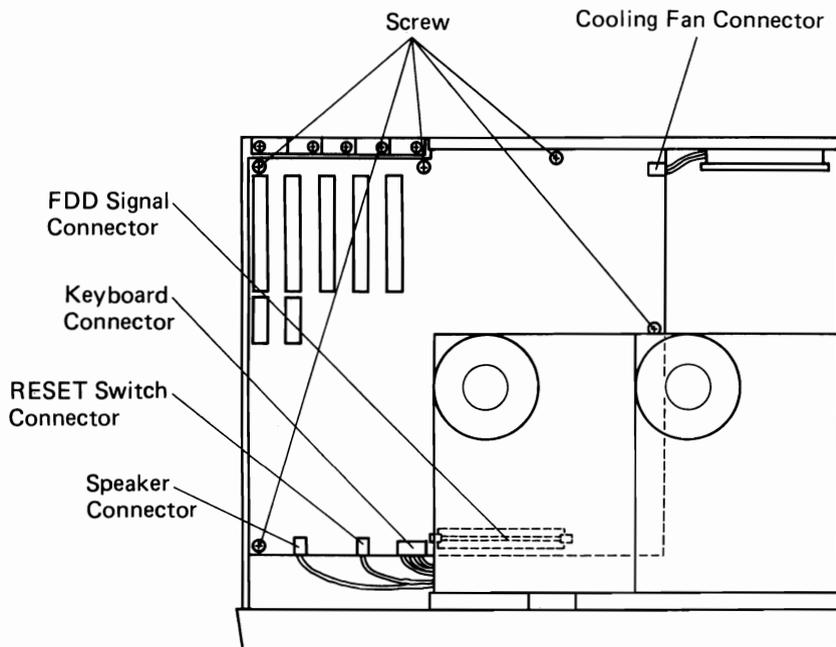


Figure 3-8

5. Remove five screws securing the main P.C.B. to the chassis.
6. Move the main P.C.B toward the front panel slightly, lift the left side of P.C.B. and remove it away from the chassis.

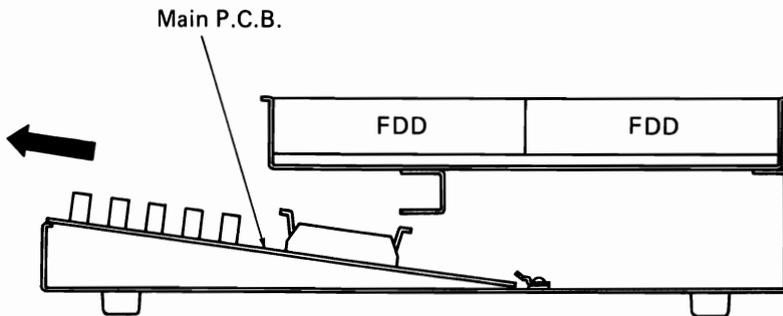


Figure 3-9

III-1-4. Floppy Disk Drive Unit

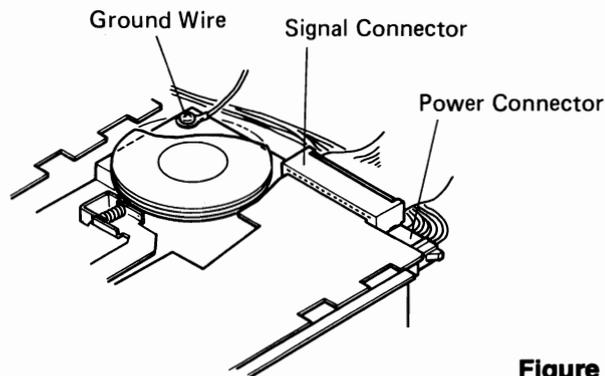


Figure 3-10

1. Disconnect the signal and power cables from the FDD (Floppy Disk Drive). On the body of the A-drive FDD, the ground wire is secured. Disconnect it by removing the screw.

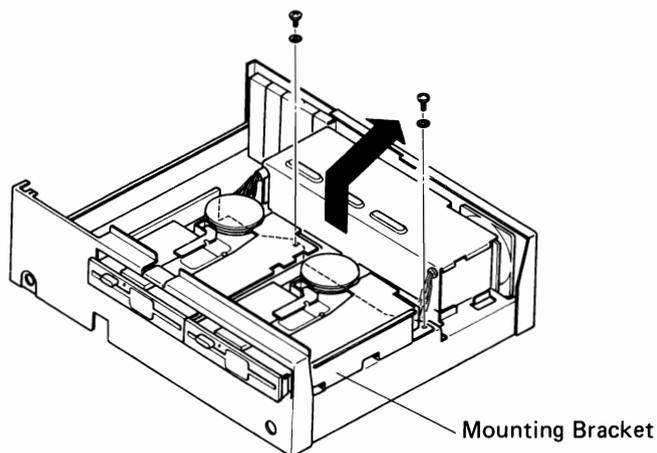


Figure 3-11

2. FDDs are mounted on the bracket. Remove two screws securing that bracket to the chassis.
3. Lift the bracket with FDDs away from the chassis. In this case, be careful not to touch internal electrical or mechanical elements on the FDDs.

III-1-5. Keyboard Unit

1. Remove two screws from the bottom of the keyboard unit.
2. Remove the rear of the top case by lifting it slightly and then remove both side of it. Be careful not to snap off the tabs of the bottom case.
3. Pull the top case toward you slightly to free it.

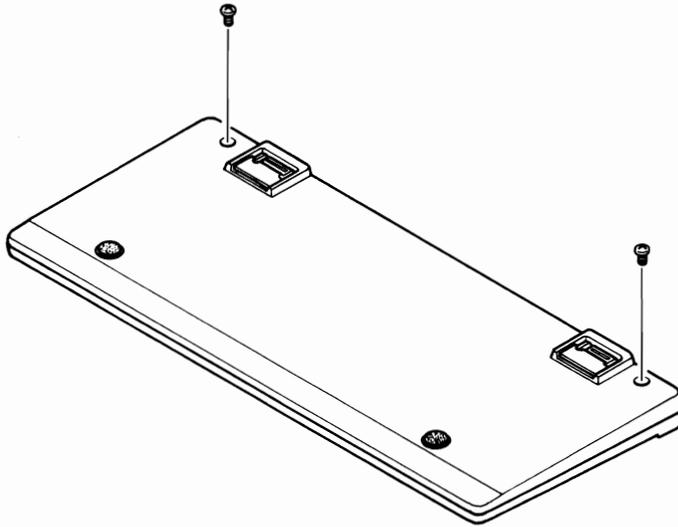


Figure 3-12

4. Remove the screw securing the ground wire to the keyboard base.
5. Lift the keyboard with the P.C.B. and coiled cable.

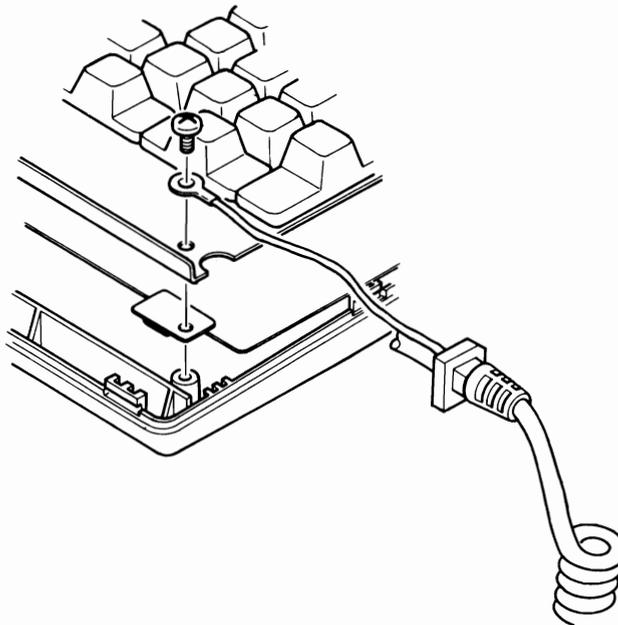


Figure 3-13

PART IV

INSTALLATION

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IV-1. Unpacking

Open the package and take out the A-200 Personal Computer.

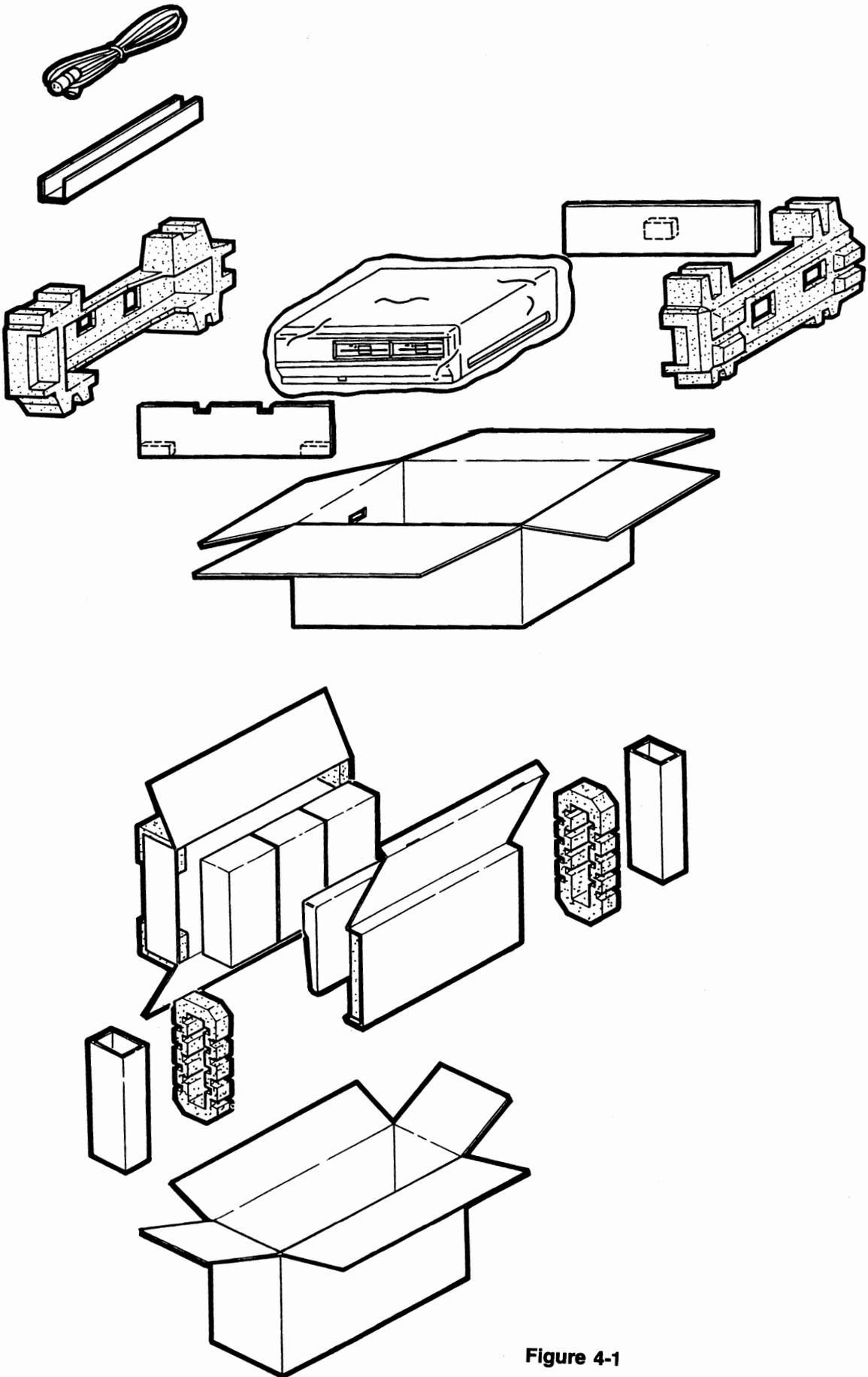


Figure 4-1

IV-2. Connections

IV-2-1. Keyboard Connection

Connect the keyboard unit to the main unit with the coiled cable.

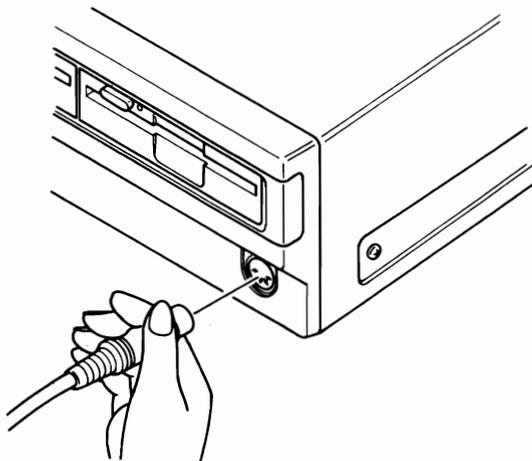


Figure 4-2

IV-2-2. AC Power Cord Connection

Insert the AC power cord with a jack into the AC power inlet located on the rear panel of the unit. In order to avoid an electric shock, be sure to insert the cord into this inlet first. Then plug the cord into a wall outlet.

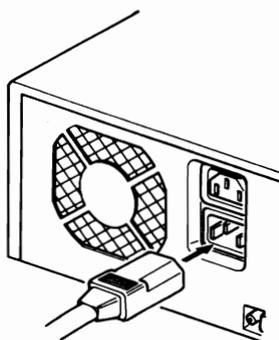
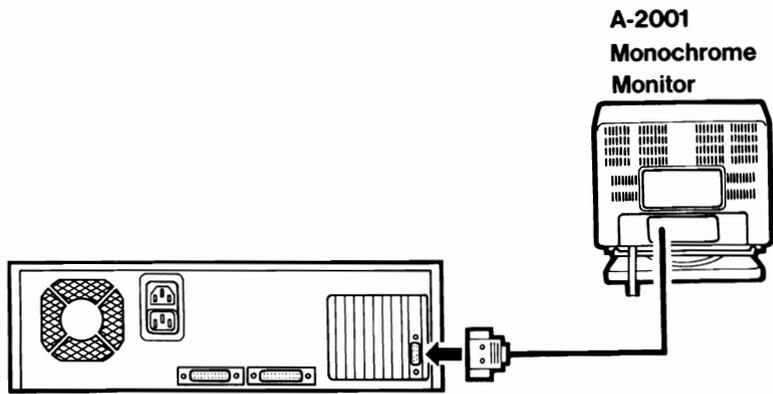


Figure 4-3

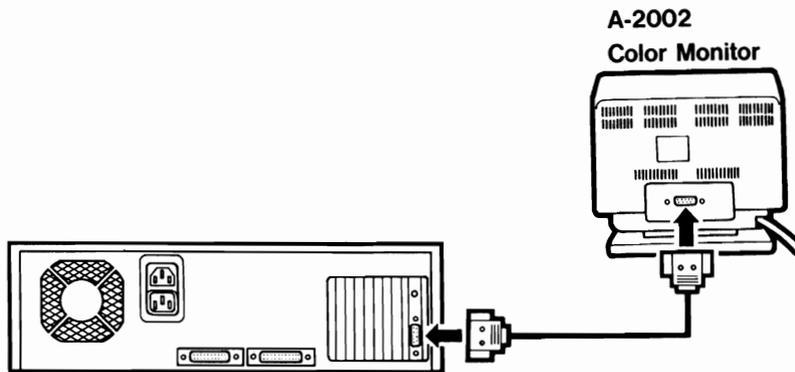
IV-2-3. Connection to Peripherals

Referring to an instruction manual supplied with your peripherals, connect them to the A-200 correctly.

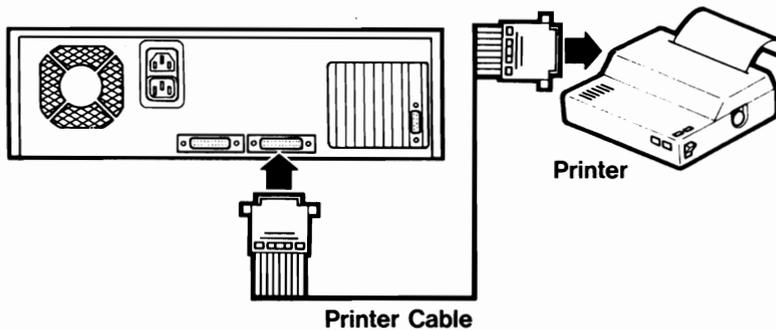
Following illustrations on connecting display monitors show connections with the Canon A-2001 monochrome monitor and the A-2002 color monitor.



Monochrome Monitor Connection



Color Monitor Connection



Printer Connection

Figure 4-4

IV-2-4. Adjustment of Typing Angle

The keyboard can be tilted for user's typing comfort. Raise the legs located at the both corner on the bottom of the keyboard unit to tilt the keyboard.

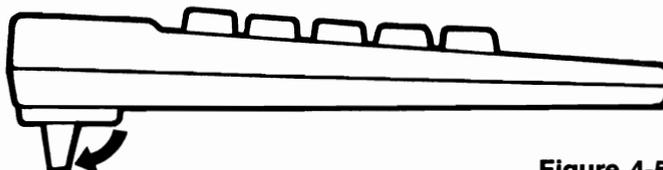


Figure 4-5

IV-3. Options

Most of options designed for IBM® Personal Computer™ such as display monitors, printers or expansion boards can also be used with the A-200.

In this part, we will give a summarized description on how to add these optional boards or integrated circuit.

Whenever an optional device to be installed inside the computer is added, settings for the DIP switch must be changed. Detailed information concerning the DIP switch is described in the next section in this part.

IV-3-1. Expansion RAM Board

The expansion RAM board supplied by Canon has 256K bytes of memory capacity. Followings are the description concerning installation for our memory expansion board.

Caution

Before installing the memory board, be sure to turn the power of the computer off, and to unplug the AC power cord from the outlet.

Insert the connectors of the expansion board into the option slot on the main circuit board of the computer. Make sure that two connectors on the expansion board are fully and firmly inserted into the slot.

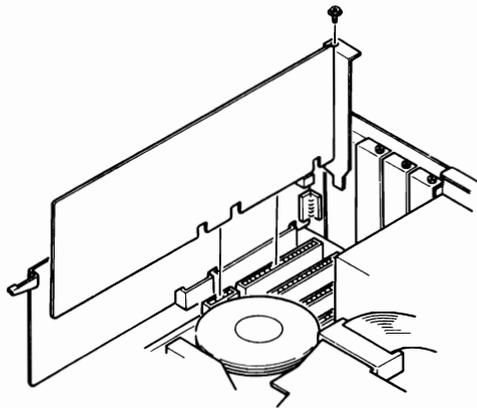


Figure 4-6

IV-3-2. Color Display Adapter Board

Whenever a user wants to upgrade the computer from Monochrome to Color system, replace the built-in monochrome adapter board with the color display adapter board. When replacing, first remove the monochrome adapter board from the leftmost slots and install this color board instead.

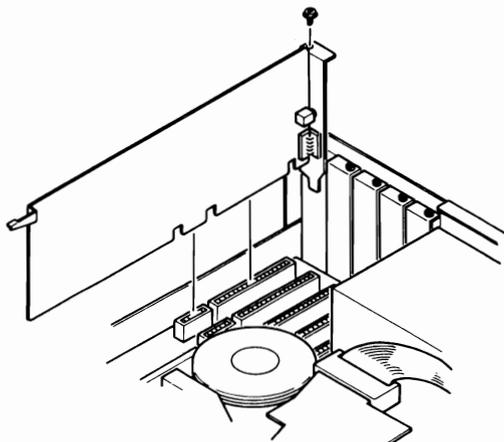


Figure 4-7

IV-3-3. NDC (8087)

NDC is an abbreviation of Numeric Data Coprocessor. When this LSI is used with the 8086 CPU, the performance of data processing will be dramatically enhanced. To achieve this, a special software is required. Installation for this LSI is very simple. The IC socket for this coprocessor is already provided adjacent to the CPU. Insert the 8087 into this socket.

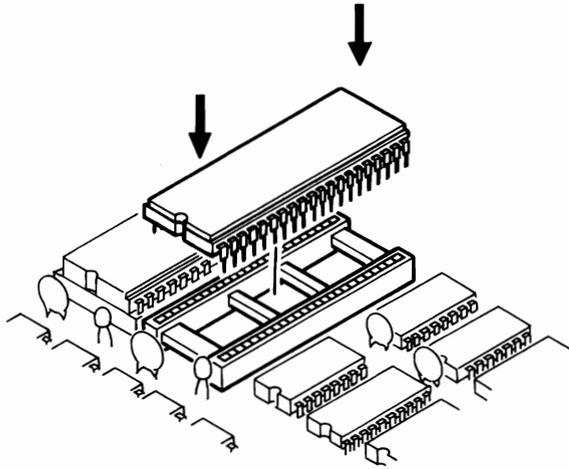


Figure 4-8

IV-4. Summary of DIP Switch Setting

IV-4-1. Main Board

On the main board, there are two DIP switches. One has 8 elements and the other has 6 elements.

- S1 (8 elements)

Bit	Function
1	For optional RAMs
2	
3	
4	
5	For optional 8087 coprocessor
6	For information to be displayed on the screen
7	
8	For the number of FDD

Table 4-1

- Settings for Optional RAMs (bit 1 through bit 4)

The upper 4 bits of this DIP switch must be set according to an answer of the following expression.

$$\frac{\text{Total RAM capacity in byte} - 64\text{K bytes}}{32\text{K bytes}}$$

For example, if total 512K bytes of RAM are installed:

$$\frac{512\text{K} - 64\text{K}}{32\text{K}} = 14 = \text{E in hexadecimal}$$

and actual settings are illustrated as follows.



Figure 4-9

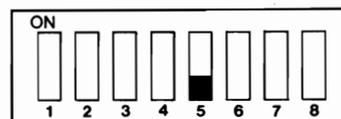
Note: If all of these switches are set to OFF position, the software automatically searches the actual amount of RAM installed, and adjust usable RAM area to that amount. The software supports in maximum of 640K bytes RAM.

- Setting for 8087 (bit 5)

When this optional LSI is installed, this bit should be reset from ON to OFF.



Not installed



Installed

Figure 4-10

- **Setting for Display Type (bit 6 and bit 7)**

These bits determine the type of display on the screen.

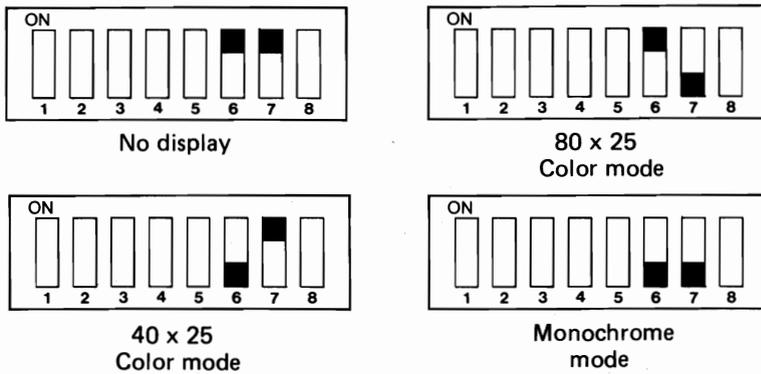


Figure 4-11

- **Setting for Number of FDD (bit 8)**

This bit should be correctly set according to the number of the floppy disk drive.

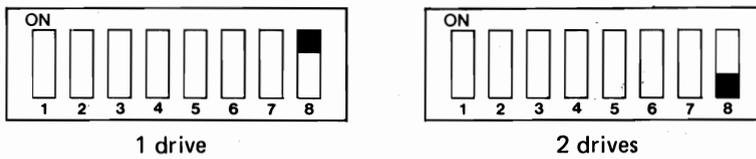


Figure 4-12

- **S2 (6 elements)**

Bit	Function
1	For RS-232C interface
2	For printer interface
3	Not used
4	For RS-232C interface
5	For printer interface
6	Not used (should always be off)

Table 4-2

The A-200 is equipped with the RS-232C interface and the printer interface on the main P.C.B., however, an extra interface board can also be used by resetting the elements of this DIP switch.

- **Settings for Additional RS-232C Board (bit 1 and bit 4)**

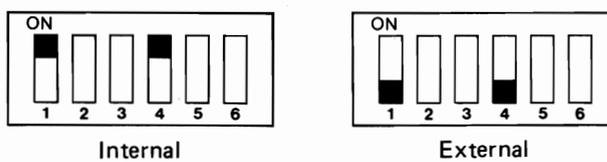


Figure 4-13

- Settings for Additional Printer Interface (bit 2 and bit 5)

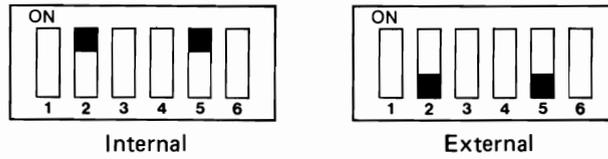
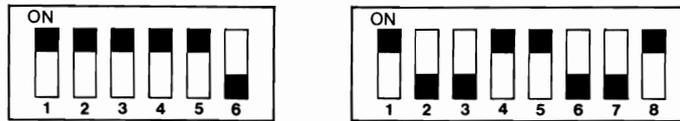


Figure 4-14

IV-4-2. DIP Switch Settings at Our Factory

There are four versions for the A-200 in its display type and number of disk drive. At the time when the computer is shipped from the factory, each element (bit) of the DIP switches have been set as shown in the following illustrations.

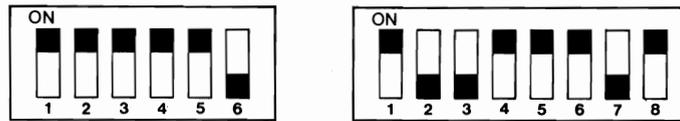
Model M1



Model M2



Model C1



Model C2

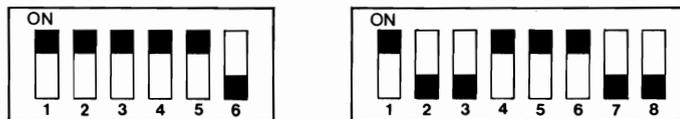


Figure 4-15

IV-4-3. Optional RAM Board

An usable address area of this RAM board can be varied by resetting the DIP switch on this board.

Bit	Usable memory area
1	40000H — 5FFFFH
2	60000H — 7FFFFH
3	80000H — 9FFFFH
4	40000H — 5FFFFH
5	60000H — 7FFFFH
6	80000H — 9FFFFH

Table 4-3

- Example 1) Usable area: 40000H - 7FFFFH



Figure 4-16

- Example 2) Usable area: 60000H - 9FFFFH

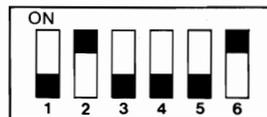


Figure 4-17

IV-5. Adding Optional Floppy Disk Drive

1. Remove the signal cable and power cable from the "Drive-A" FDD. Disconnect the ground wire from the body of the FDD by removing the screw.

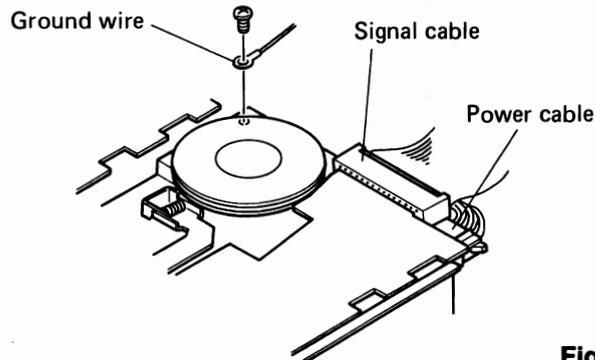


Figure 4-18

2. A power supply cable for an additional FDD is already prepared on the mounting bracket of the FDD. Remove it from the bracket by removing the nylon binder.

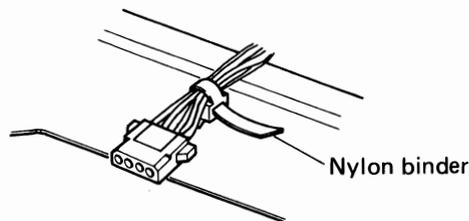


Figure 4-19

3. Disconnect the signal cables with connector from the main P.C.B. To disconnect, rotate the two hooks outwards.

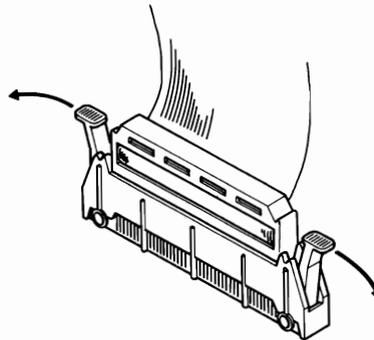


Figure 4-20

4. Remove the FDD with bracket by referring to the paragraph "Floppy Disk Drive Removal".
5. Remove the hook of the clamber for the additional signal cables through the hole of the bracket. In this case apply force to the both sides of the hook and push out the clamber. Then remove the cables away from the clamber.

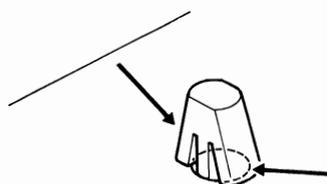


Figure 4-21

6. Remove the pocket by pulling it toward you.

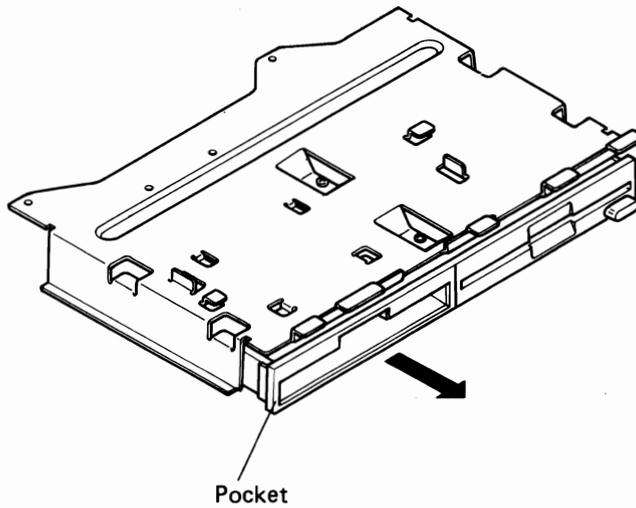


Figure 4-22

7. Disconnect the plug of the drive selector on the additional FDD and reinsert it into "S2" pins. This defines it as the "Drive-B" FDD.

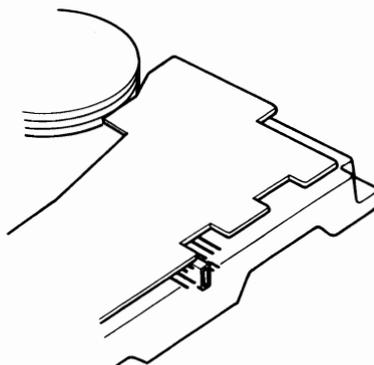


Figure 4-23

8. Turn the mounting bracket upside down and secure the optional FDD with four screws.

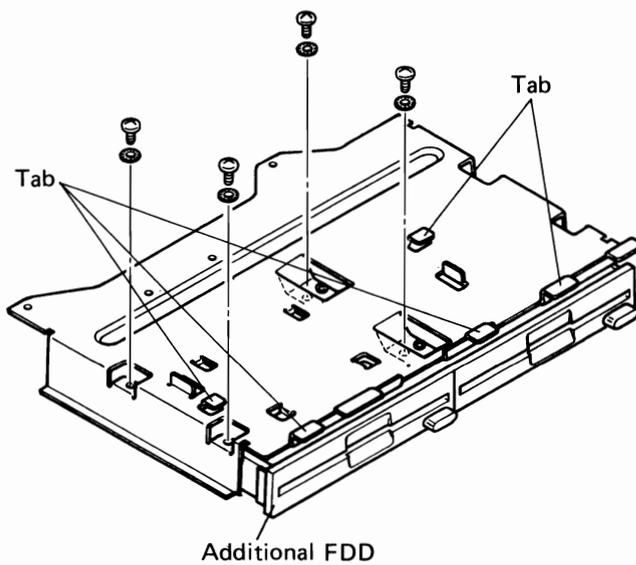


Figure 4-24

9. Position the bracket with FDDs on the chassis. Slide it toward you until the tabs of the bracket are inserted into the holes on the front of the chassis.
10. Secure the bracket to the chassis using two screws.
11. Insert the connector of the signal cables into the connector on the main P.C.B.

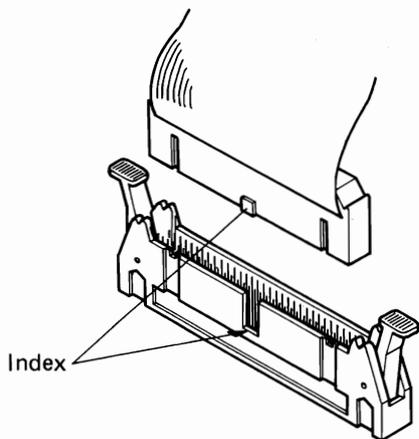


Figure 4-25

12. Connect the signal cables and power cables to both FDDs.

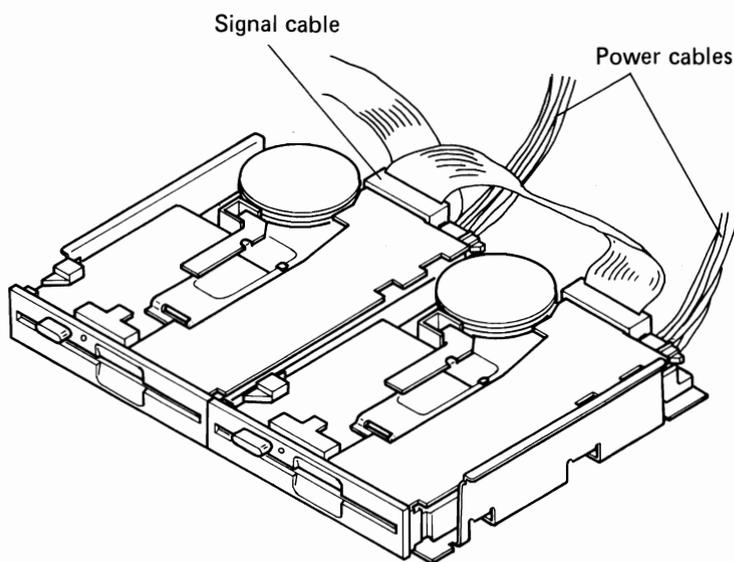


Figure 4-26

PART V

ADJUSTMENT

CONTENTS

V-1. System Clock	39
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V-1. System Clock

1. Connect the frequency counter to pin-12 (OSC) of U125 (CG) on the Main P.C.B.
2. Adjust CT1 trimmer capacitor to read 14.31818MHz on the frequency counter.

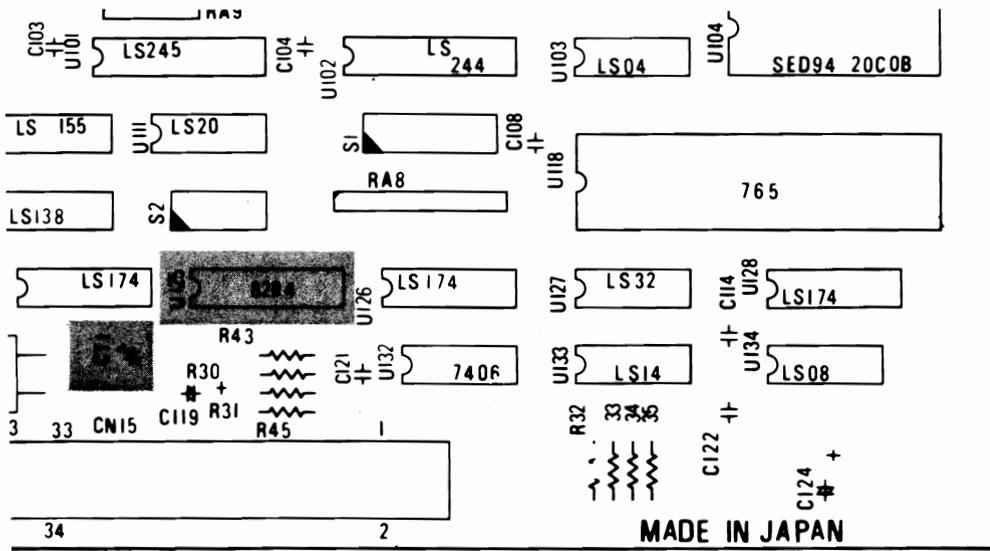


Figure 5-1

V-2. +5V Power Supply

1. Connect the DC voltmeter to pin-5 or 6 (RED) of CN9 on the Main P.C.B.
2. Adjust VR1 on the power supply P.C.B. to read +5V \pm 0.05V on the DC voltmeter.

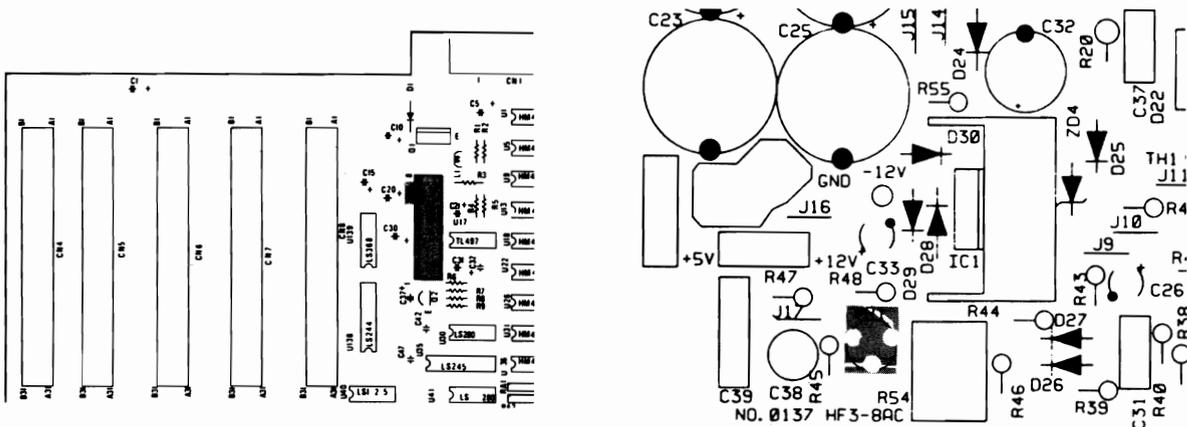


Figure 5-2

PART VI

THEORY OF OPERATIONS

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VI-1. General

Figure 6-1 shows a typical system configuration of the A-200 and peripherals. As this figure shows, the A-200 is constructed by the main P.C.B., power supply, monochrome display adapter board or color display adapter board, one or two floppy disk drive unit(s) and keyboard.

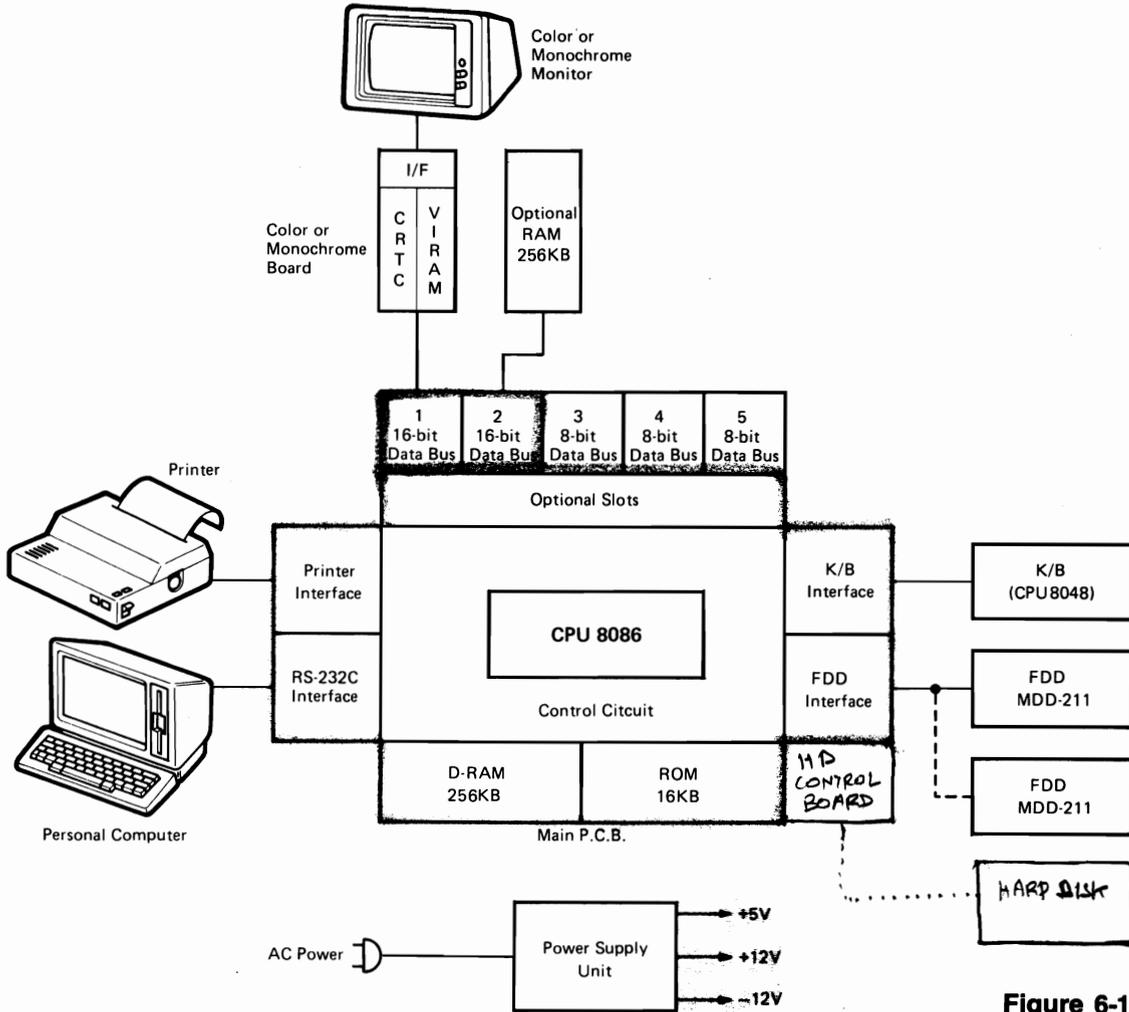


Figure 6-1

The main P.C.B. consists of the 8086 16-bit microprocessor, 256K bytes of system RAM, 16K-byte ROM which contains the power-on diagnostic program, BIOS and IPL (initial program loader), the printer interface, asynchronous communication interface, keyboard interface, floppy disk drive interface. Another various control circuits are also equipped with the computer in order to work these elements effectively.

The power supply unit outputs three different power sources — +5V 8.5A, +12V 2.0A and -12V 0.3A. Output voltages are stabilized with the switching regulator, therefore this unit takes less space and is light-weight.

The monochrome display adapter board uses the 68B45 LSI as CRTC (Cathode-Ray Tube Controller). The 4K bytes of static RAMs are used as video-RAM (V-RAM) which supports one screen of 25 rows × 80 characters and attribute. The 256 characters to be displayed on the screen are involved into the 8K-byte ROM. Output signals such as intensity signal, horizontal drive signal and vertical drive signal are sent from the 9-pin connector mounted on this display board.

The color display adapter board also uses the 68B45 as CRTC. On this board, 32K bytes of dynamic RAMs are installed. These RAMs supports 40 × 25 characters or 80 × 25 characters of text screen and 320 × 200 pixels or 640 × 200 pixels of graphics.

Like the monochrome display adapter board, this board also has the 9-pin connector, however its pin assignment is different.

This connector outputs various video signals such as RED, GREEN and BLUE color signals, intensity signal, horizontal drive signal and vertical drive signal.

In addition to this 9-pin connector, the color display adapter board has an RCA-type jack which outputs video composite signal.

The A-200 is equipped with one or two Canon MDD-211 5-1/4" floppy disk drive(s). Please refer to separate MDD-221/211 WORKSHOP MANUAL (SY8-0031-721) for any further information on this disk drive.

The keyboard can be connected to the main unit by means of a 5-pin DIN type connector with a coiled cable. The 8048 one chip microprocessor is mounted on the internal circuit board of the keyboard. This processor is used as an interface with the keyboard and the CPU. When the power for the A-200 is turned on, this processor automatically checks its own RAM or stuck keys by executing the self diagnostic program.

In this part, we have divided the circuit of A-200 into the following four sections:

- Main P.C.B.
- Keyboard unit
- Display adapter boards
- Power supply unit

VI-2. Main P.C.B.

Figure 6-2 illustrates the block diagram for the main P.C.B. Followings are the descriptions for the LSIs used in the A-200. We will use abbreviations hereinafter when describing about these LSIs.

- **CPU (Central Processing Unit): 8086**

16-bit microprocessor; it can access 1M bytes of memory address and 64K bytes of I/O address directly.

- **NDC (Numeric Data Coprocessor): 8087**

This optional LSI is a coprocessor for performing arithmetic operations. The 8087 is to be installed into the internal 40-pin IC socket with an user's request.

- **DMAC (Direct Memory Access Controller): 8237**

Control data transfer between I/O devices which are connected to the DMA channels and memory without CPU intervention.

The 8237 refreshes dynamic RAMs on the main P.C.B. and ones on the optional boards inserted into the optional slots.

- **BCU (Bus Control Unit): 8288**

This generates signals necessary for controlling I/O devices and memory by receiving the SO, S1 and S2 status signals from the CPU.

- **PIC (Programmable Interrupt Controller): 8259**

Accepts interrupt signals from the I/O devices, and gives priority to one of them. The interrupt signal selected by the 8259 is sent to the CPU.

- **PPI (Programmable Peripheral Interface): 8255**

It has three sets of 8-bit input/output ports, and accesses data input from the keyboard or data set by the DIP switches.

- **UART (Universal Asynchronous Receiver/Transmitter): 8250**

Controls the RS-232C interface. Parameters for communication such as baud rate, word length, stop bit and parity can be controlled by the CPU through this LSI.

- **FDC (Floppy Disk Drive Controller): 765**

Controls the built-in one or two floppy disk drive(s).

- **CG (Clock Generator): 8284**

Generates clock signals necessary for the computer. The 8284 also synchronizes the READY signal with the CLK signal to be sent to the CPU.

- **ROM (Read Only Memory): 2764**

The A-200 uses two P-ROMs whose respective storage capacity is 8192 words \times 8 bits. They contain power-on self diagnostic program, BIOS, dot patterns for 128 characters in graphics mode and floppy disk bootstrap loader.

- **PIT (Programmable Interval Timer): 8253**

Generates an interruption signal when the predetermined timer becomes active and determines frequency of a signal to be sent to the speaker.

- **RAM (Random Access Memory)**

On the main P.C.B, there are 36 dynamic RAMs whose respective storage capacity is 65536 words \times 1 bit.

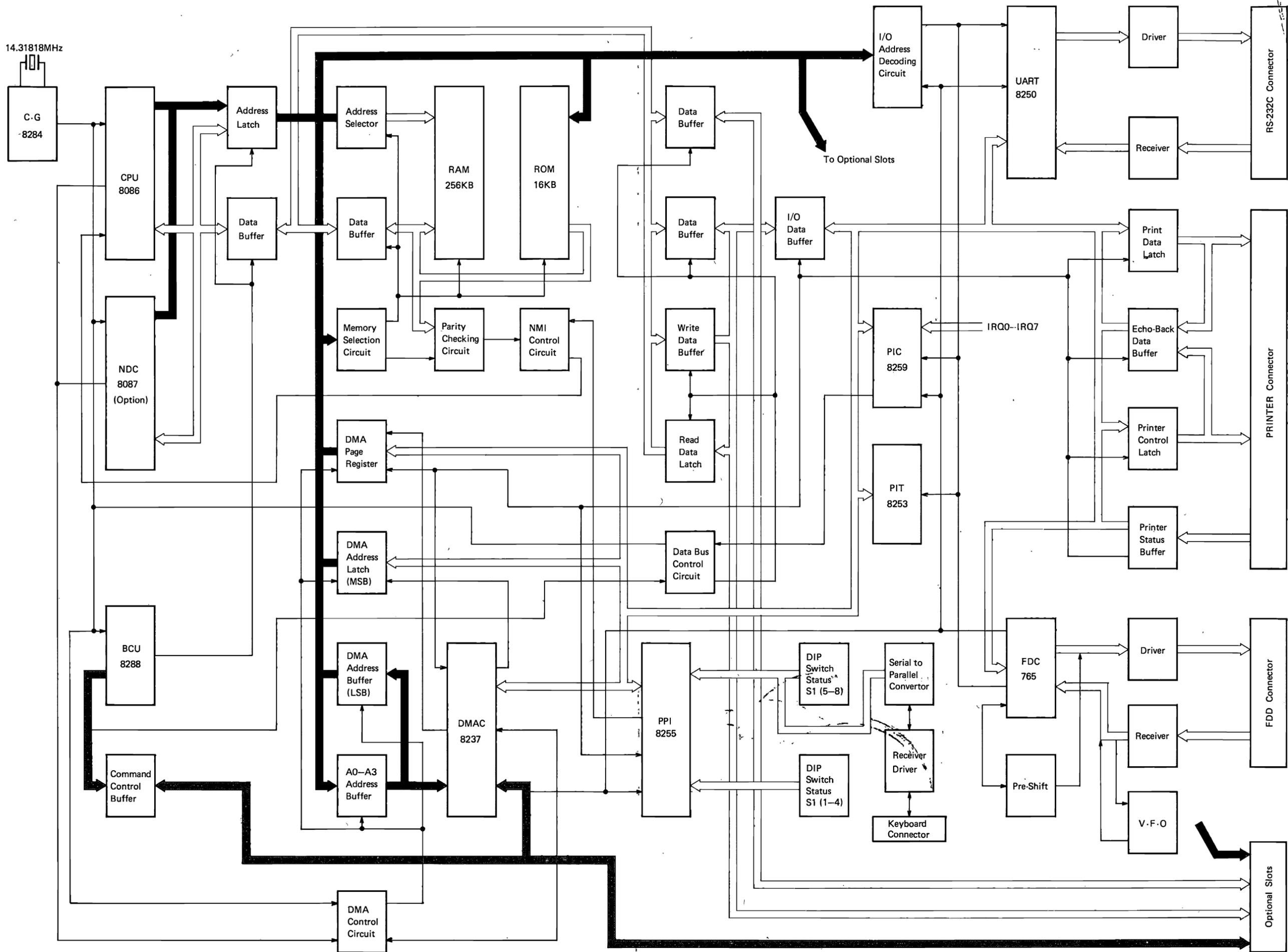
Every one byte (8 bits) of data has one parity bit and therefore, actually 32 of 36 RAMs are used as system memory. So,

$64\text{K-bit} \times 32 \text{ peaces} = 2048\text{K bits} = 256\text{K bytes}$

of storage capacity are available.

Above LSIs are connected to the address bus, data bus and control bus so as to synchronize their functions effectively, and are controlled by the CPU directly or indirectly.

At the same time, the signals through these buses are sent to the optional slots and control the monochrome or color display adapter board or any other option boards.



14.31818MHz

C.G.
8284

CPU
8086

NDC
8087
(Option)

BCU
8288

Command
Control
Buffer

Address
Latch

Data
Buffer

Address
Selector

Data
Buffer

Memory
Selection
Circuit

DMA
Page
Register

DMA
Address
Latch
(MSB)

DMA
Address
Buffer
(LSB)

A0-A3
Address
Buffer

DMA
Control
Circuit

RAM
256KB

ROM
16KB

Parity
Checking
Circuit

NMI
Control
Circuit

DMA
Control
Circuit

DMAC
8237

Data
Buffer

Data
Buffer

Write
Data
Buffer

Read
Data
Latch

Data Bus
Control
Circuit

I/O
Address
Decoding
Circuit

To Optional Slots

I/O
Data
Buffer

PIC
8259

PIT
8253

PPI
8255

DIP
Switch
Status
S1 (5-8)

Serial to
Parallel
Convertor

FDC
765

DIP
Switch
Status
S1 (1-4)

Receiver
Driver

Pre-Shift

UART
8250

Driver

Receiver

Print
Data
Latch

Echo-Back
Data
Buffer

Printer
Control
Latch

Printer
Status
Buffer

Driver

Receiver

V.F.O.

RS-232C
Connector

PRINTER
Connector

FDD
Connector

Optional
Slots

VI-2-1. CPU

The A-200 uses the 8086 16-bit microprocessor in maximum mode.

Figure 6-3 shows the pin assignment and pin description for the 8086 operated in maximum mode.

- **AD15 — AD0 (Address and Data) inputs/outputs in three states**

These lines construct the memory and I/O address bus (T1) and the data bus (T2, T3, TW, T4). The A0 signal acts similar to the $\overline{\text{BHE}}$ signal to the lower byte (D0 — D7) data bus. If one byte is to be sent to the lower bytes of the bus in memory access or I/O control operation, the A0 terminal becomes LOW during the period of T1.

These terminals keep high impedance during interrupt acknowledge and hold acknowledge cycle of local bus.

- **A19/S6, A18/S5, A17/S4, A16/S3 (Address/Status) outputs in three states**

These lines output upper 4 bits of data in memory accessing during the period of T1. When I/O operation, these lines are all LOW. During T2, T3, TW and T4 in memory access or I/O control operation, a status information is output. The status of the interrupt enable flag 1F (S5) is reset with the beginning of each CLK cycle (T1). S6 is always zero.

A17/S4, A16/S3 are encoded as follows:

A17/S4	A16/S3	
0	0	Alternate Data
0	1	Stack
1	0	Code or None
1	1	Data

Above information shows which relocation register is used for data accessing. Impedance of these lines keep high during hold acknowledge cycle of the local bus.

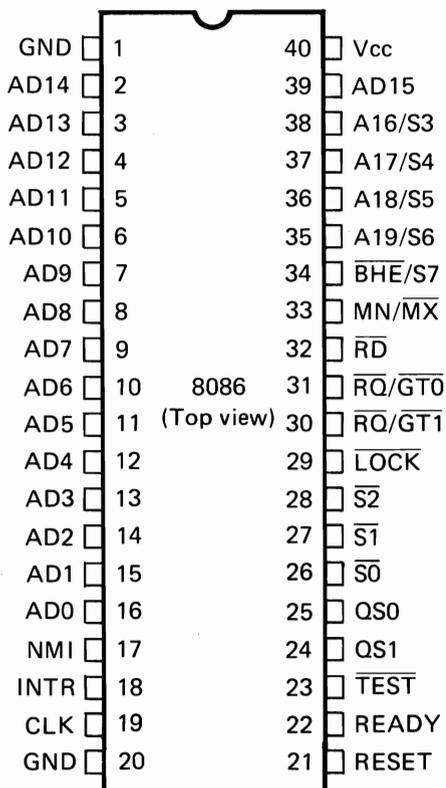


Figure 6-3

- **$\overline{\text{BHE}}/\text{S7}$ (Bus High Enable/Status) output in three states**

During T1, the $\overline{\text{BHE}}$ signal is used to permit the upper half of the data bus (D15 — D8) to output data. An 8-bit type device connected to the upper half of the bus uses the $\overline{\text{BHE}}$ signal for chip selecting purpose.

When one byte is sent at the upper half of the bus, $\overline{\text{BHE}}$ becomes LOW during read, write and interrupt acknowledge cycle.

S7 status information will yield during the period of T2, T3 and T4. The $\overline{\text{BHE}}$ signal is active LOW and its impedance is high during hold acknowledge cycle of the local bus. This signal becomes LOW during T1 of the interrupt acknowledge cycle.

- **$\overline{\text{RD}}$ (Read Strobe) output in three states**

This signal indicates that the CPU is now executing memory read ($\overline{\text{S2}}=1$) or I/O read ($\overline{\text{S2}}=0$) cycle. The $\overline{\text{RD}}$ signal is used to read devices which are connected on the 8086 local bus line. This $\overline{\text{RD}}$ signal keeps active LOW during memory read cycle T2, T3 and TW. At T2, until the 8086 local bus's impedance becomes high, the $\overline{\text{RD}}$ remains HIGH.

This signal becomes high impedance during the hold acknowledge cycle of the local bus.

- **READY (Ready) input**

This acknowledgement signal denotes that the data transfer has been completed, and are sent from memory or I/O devices which CPU has been addressed.

The RDY signal from memory or I/O devices will become the READY signal synchronized with the CLK signal by the CG.

- **INTR (Interrupt Request) input**

This signal is a trigger input sampled between the last clock cycle of each instruction in order for the CPU to determine whether the interrupt acknowledge operation is performed or not. One subroutine is assigned through one interrupt vector lookup table which is located on the system memory.

The INTR signal can be internally masked by resetting the interrupt enable flag (IF) with the software. This signal is active HIGH.

- **NMI (Non Maskable Interrupt) input**

The NMI signal is an edge trigger input which causes the type-2 interrupt. One subroutine is assigned through one interrupt vector lookup table which is located on the system memory. This signal cannot be masked by the software. If there is a raising edge from LOW to HIGH, an interruption will occur after an instruction currently executing is completed.

As for the A-200, a memory parity error gated with the NMIEN signal and the interrupt signal for the NDC are input to the CPU.

- **RESET (Reset) input**

This signal terminates the operation of the CPU immediately. The RESET signal must be kept HIGH for at least four clock cycles. When the RESET signal returns to LOW, the CPU outputs the first address (FFFF0H) and then restarts executing after 10 clock cycles has been passed.

- **CLK (Clock) input**

This clock supplies the fundamental timing signal to the CPU. In order to obtain optimum internal timing, the CLK must be an asymmetric wave with 33% of duty cycle.

This clock signal is obtained by dividing the 14.31818MHz fundamental clock by three with the 8284 clock generator.

- **$\text{MN}/\overline{\text{MX}}$ input**

This terminal determines whether the 8086 is operated in minimum mode or maximum mode. In this computer, the CPU is operated in maximum mode and to achieve this, this terminal is connected to the ground.

- $\overline{\text{LOCK}}$ (Lock) output in three states

The $\overline{\text{LOCK}}$ signal denotes that the CPU cannot be controlled by the system bus during another system bus master or $\overline{\text{LOCK}}$ signal is active (LOW). This signal becomes active with the prepositioned "LOCK" instruction and remains active until the execution of the next one instruction has been completed. This signal's impedance keeps high during local bus's hold acknowledgement.

- QS1, QS0 (Queue Status) outputs

These signals output the status of the instruction queue to the 8087 NDC.

QS1	QS0	
0	0	No operation (queue is not changed)
0	1	Indicates that the queue is the first byte of the ope-code.
1	0	Indicates that the queue register is empty.
1	1	Indicates that the queue is the second or upper byte of the instruction.

These signals are effective during next clock cycle of when the queue operation has been executed.

- $\overline{\text{S2}}$, $\overline{\text{S1}}$, $\overline{\text{S0}}$ (Status) outputs in three states

These status signals are encoded as follows

$\overline{\text{S2}}$	$\overline{\text{S1}}$	$\overline{\text{S0}}$	
0	0	0	Interrupt acknowledge
0	0	1	Read I/O ports
0	1	0	Write I/O ports
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

These status signals become active during the period of T4, T1 and T2, and return to passive (111) condition during TW.

These signals are used by the BCU to generate all the memory and I/O signals. A change of $\overline{\text{S2}}$, $\overline{\text{S1}}$ and $\overline{\text{S0}}$ at the period of T4 is used to indicate the beginning of the bus cycle, and a passive state of the bus at T3 or TW is used to indicate the end of the bus cycle.

These signal's impedance will remain high during hold acknowledge cycle of the local bus.

- $\overline{\text{RQ/GT0}}$, TEST

These terminals are not used and therefore are pulled up to the power supply line (Vcc).

- $\overline{\text{RQ/GT1}}$

This terminal is connected to the $\overline{\text{RQ/GT0}}$ terminal of the NDC for the purpose of multi-bus operation.

VI-2-2. RESET Signal and Clock Generator Circuit

Figure 6-4 shows the RESET signal and clock generator circuit. The LSI 8284 is the heart of this circuit. It generates RESET, CLK, PCLK, READY and OSC signals.

The RESET signal is generated by detecting a rising up of Vcc connected to the $\overline{\text{RES}}$ terminal, and is sent to the CPU, each device and option slots. This signal is also generated by pushing the RESET switch located on the front panel.

The diode MA150 is used to discharge the 47-micro-farad capacitor.

The CLK signal is obtained by dividing by three the fundamental clock, generated by the 14.31818MHz quartz crystal connected to this IC. This signal is sent to the CPU and constructed the duty ratio as shown in Figure 6-5.

The PCLK signal is made by dividing the CLK signal into the half and used as the clock input for the timer circuit or the timing clock for the keyboard interface.

The OSC signal is 14.31818MHz clock and sent to the monochrome board or color board through the option slots.

The READY signal indicates that one instruction cycle of the CPU has been completed. This signal is made from the $\overline{AEN1}$ and RDY1 signals. The READY signal is cleared after the guaranteed hold time to the CPU has been met.

DCLK is made from the OSC and CLK signals and used as a clock signal for the 8237 (DMAC).

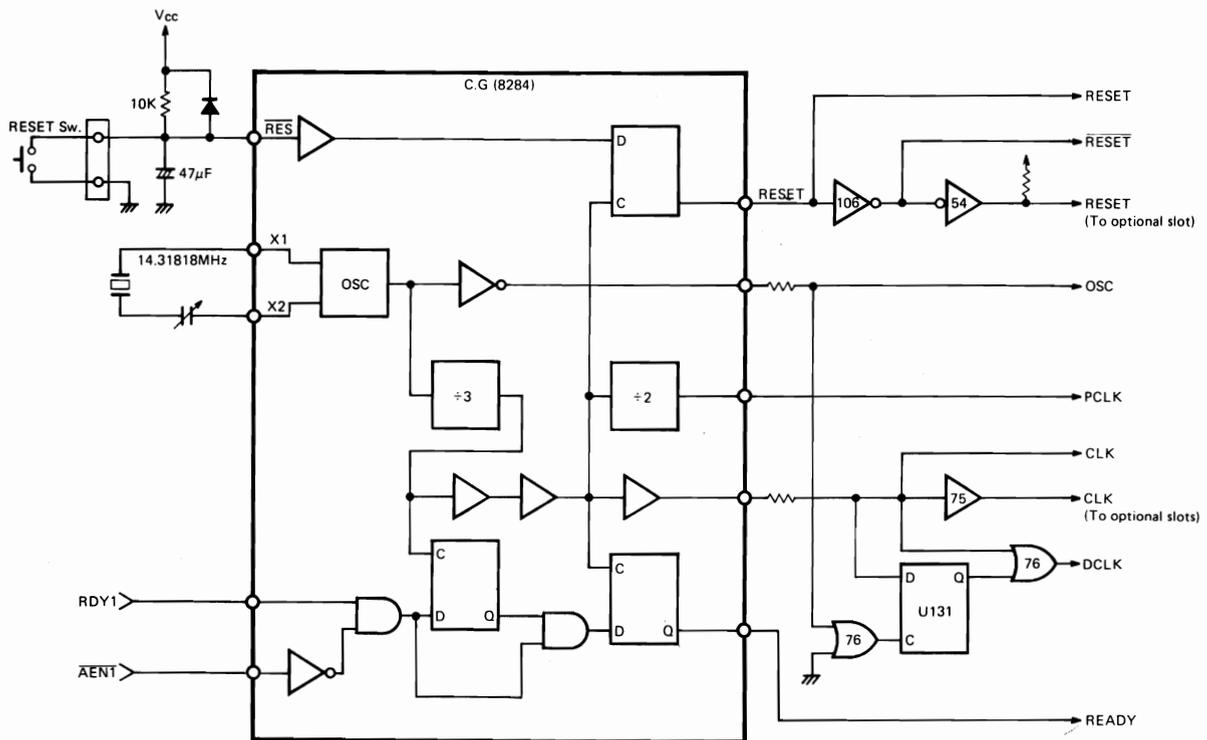


Figure 6-4

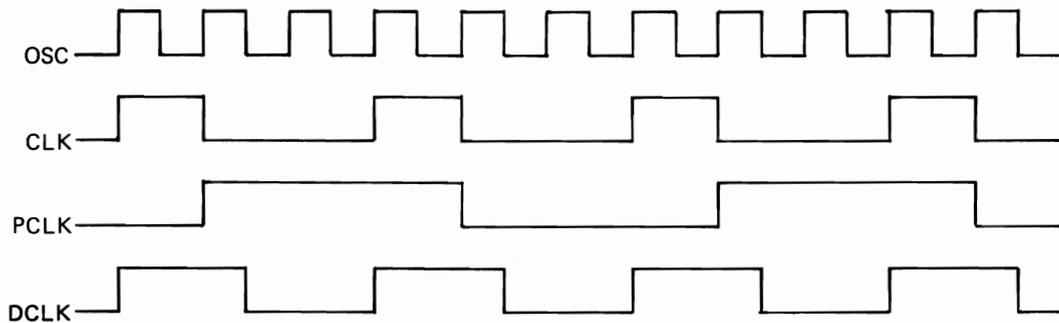


Figure 6-5

VI-2-3. NMI and INT Control Circuit

The 8086 has two interrupt terminals. One is the NMI (Non-maskable Interrupt) and the other is the INT (Interrupt).

In the A-200, the NMI terminal is used to detect parity error at the main RAM, parity error from the option slots and interrupt from the NDC.

The PIC sends the INT signal to the CPU after priority is given to one of the interrupt signals from the internal or external devices.

Figure 6-6 shows the interrupt control circuit and Table 6-1 shows the assignment of IRQ0 through IRQ7 signals.

Priority	Signal	Description
High ↓ Low	IRQ0	Interrupt from the timer IC (8253)
	IRQ1	Interrupt from the keyboard
	IRQ2	Interrupt from the optional slot
	IRQ3	Interrupt from the optional slot
	IRQ4	Interrupt from the USART (8250)
	IRQ5	Interrupt from the optional slot
	IRQ6	Interrupt from the FDC (μ PD765)
	IRQ7	Interrupt from the printer interface

Table 6-1

As Figure 6-6 shows, the NMI signal is ANDed with the NMIEN signal before it is sent to the CPU. This NMIEN signal is the output of the register which is assigned with the I/O address 0AXH from the CPU. The NMIEN signal is reset when the power for the computer is turned on, and when the RAM checking involved in the initial power-on diagnostic program is completed, this signal is set.

When the CPU receives this interruption, an execution jumps to the service routine having the entry address of 0008H.

When the CPU is interrupted at the INT terminal, it returns the INTA (Interrupt Acknowledge) signal to the PIC through the command bus. Then the PIC sends the vector address corresponding to the preassigned interrupted device to the CPU through the data bus.

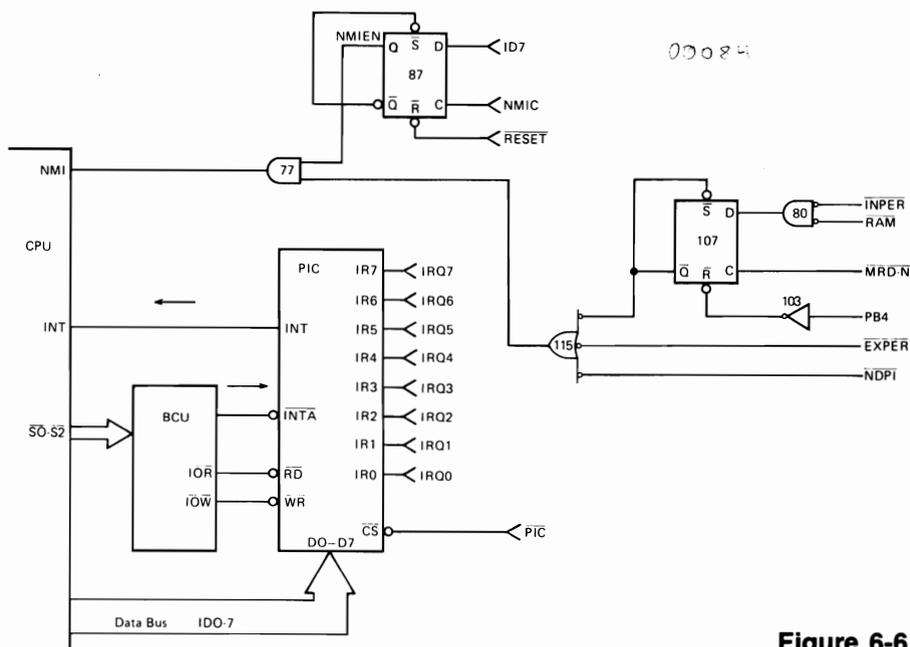


Figure 6-6

VI-2-4. Memory Map

Figure 6-7 shows the memory map for the A-200.

The CPU can access in maximum of 1M bytes of memory area directly. In the A-200, memory area is constructed by ROM, system RAM, V-RAM and optional RAM. As for the optional RAM, this figure illustrates only the 256K-byte optional RAM board supplied by Canon. The total RAM area supplied by Canon is 512K bytes (00000 to 7FFFF). However, If all of DIP switches (bit 1 through 4 of the DIP switch S1) are set to OFF position, the software automatically searches the actual amount of RAM installed, and adjust usable RAM area to that amount. The software supports in maximum of 640K bytes RAM.

Basically, the A-200 has 16-bit data bus line and therefore, physical memory chip assignment is divided into even addresses and odd addresses. As for the RAM, a parity bit is added to either one byte of even or odd address.

Since the A-200 uses the 4864 type dynamic RAMs, every one chip corresponds to every one bit of data bus.

V-RAM used in the color board is 48416 type dynamic RAMs. Every one RAM chip is assigned with every 4 bits of the data bus.

As for the monochrome board, it uses 6116 type static RAMs as V-RAM. Every one chip of RAMs corresponds to one byte of even addresses and odd addresses respectively.

Correspondence to the data bus in ROM is similar to the RAMs in the monochrome board since 2764 type P-ROM or C-MOS masked ROM is used as ROM.

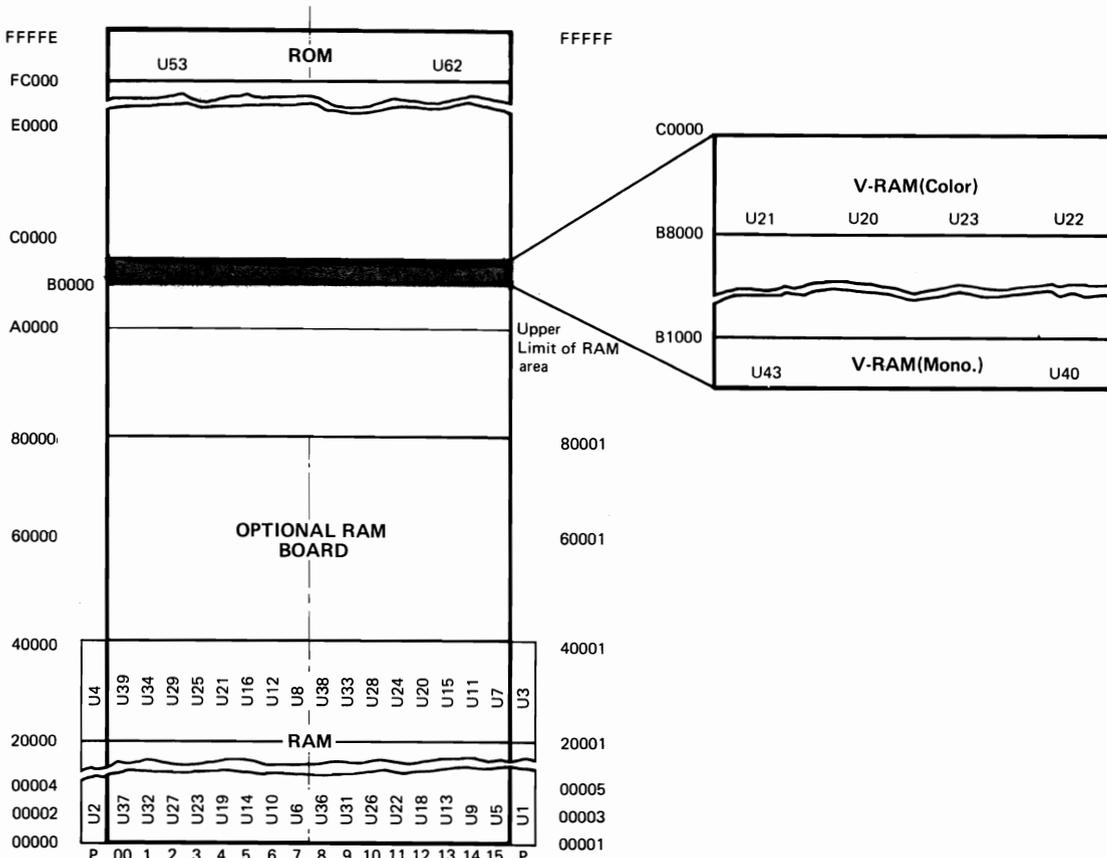


Figure 6-7

VI-2-5. Memory

On the main P.C.B. of the A-200, 256K bytes of D-RAMs and 16K bytes of ROMs are installed. In this section, we will describe on the addressing for ROM and RAM, and on how to check parity bit of RAM.

• ROM addressing

The \overline{ROM} signal output from the gate logic constructed with U85, U91 and U98 becomes LOW when the CPU accesses the memory area higher than FC000H. Next, this signal is ANDed with the \overline{BHE} signal or A0 signal.

When the CPU executes a byte transfer operation to the even addresses over FC000H, the A0 signal becomes LOW and the \overline{BHE} signal becomes HIGH, and finally, $\overline{ROME\overline{V}}$ signal will be output. Conversely, when the CPU executes a byte transfer operation to the odd addresses, the A0 becomes HIGH, the \overline{BHE} becomes LOW and then the \overline{ROMOD} signal will be output. When the CPU executes a word transfer operation to the even addresses, the A0 becomes LOW, the \overline{BHE} also becomes LOW and as a result, both the $\overline{ROME\overline{V}}$ and \overline{ROMOD} signals are output. When the $\overline{ROME\overline{V}}$ is LOW, the CPU selects the ROM U53, and when the \overline{ROMOD} is LOW, selects U62.

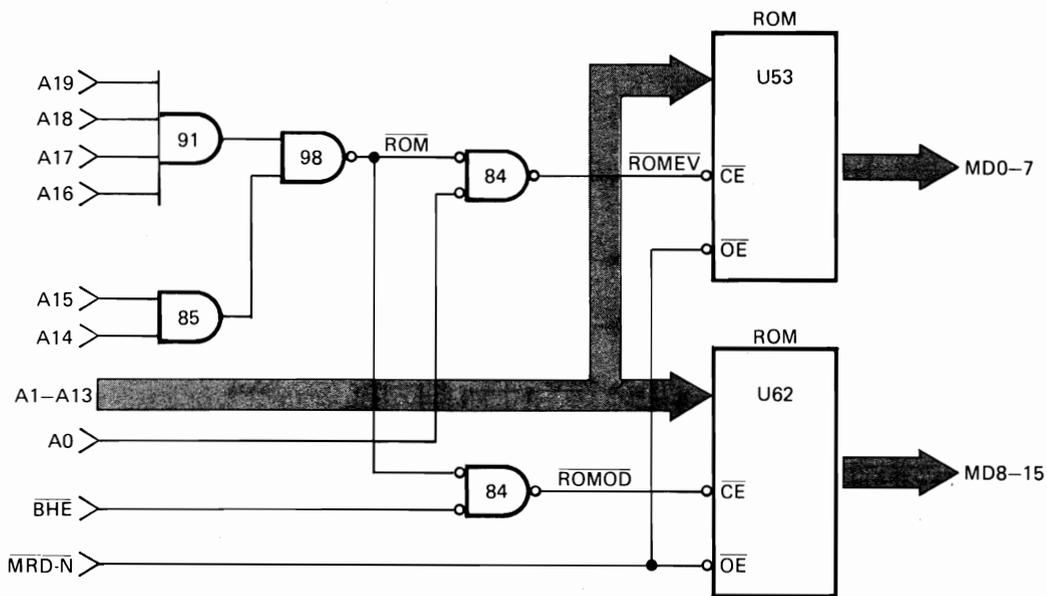


Figure 6-8

• RAM Addressing

The 36 D-RAMs installed in the A-200 are categorized into following four groups.

- * 00000H through 1FFFEH having even addresses
- * 00001H through 1FFFFH having odd addresses
- * 20000H through 3FFFEH having even addresses
- * 20001H through 3FFFFH having odd addresses

One of above four groups is selected by \overline{RAMLE} (RAM Low Even), \overline{RAMLO} (RAM Low Odd), \overline{RAMHE} (RAM High Even) and \overline{RAMHO} (RAM High Odd) signals. For example, in the case of transferring 1-byte data from the address 0000H, the \overline{RAML} signal from the Y0 terminal of U86 becomes LOW. Then this \overline{RAML} signal is ANDed with the A0 signal at U90 and further ANDed with the \overline{MRD} or \overline{MWR} signal at the U85, and finally the \overline{RAMLE} signal becomes LOW.

Since this $\overline{\text{RAMLE}}$ signal is connected to the $\overline{\text{RAS}}$ terminals of each RAM chip whose addresses is 00000H to 1FFFEH, the address signals MA0 to MA7 assign RAMs as they are of row address. These MA0 to MA7 signals are separated into row addresses and column addresses by the signal that is delayed the $\overline{\text{RAMLE}}$ signal in 20 nano seconds by DL1 (Delay Logic) at the selectors U47, U48 and U40. After 80 nano seconds when the $\overline{\text{RAMLE}}$ signal has become LOW, a HIGH level signal is output from the pin 10 of the DL1. This signal is inverted at U92, and is sent to the $\overline{\text{CAS}}$ terminal. Since the select signals of U47, U48 and U40 are already LOW, the column addresses are output to the MA0 through MA7.

Refreshment for the D-RAMs by the DMAC begins with the DMA Request signal DREQ0 generated from the PIT at every 15 micro seconds. When the DMAC receives this signal, it sets the CPU in WAIT mode, and then makes $\overline{\text{DACK0}}$ to LOW. Then U97 and U90 generate $\overline{\text{RAMLE}}$, $\overline{\text{RAMLO}}$, $\overline{\text{RAMHE}}$ and $\overline{\text{RAMHO}}$ signals from the MRD signal inverted the $\overline{\text{MRD-N}}$ signal output from DMAC and the inverted signal of $\overline{\text{DACK0}}$. Finally, DMAC outputs refresh addresses of A0 to A7 to the address bus as row addresses.

In this case, since U47 (Row/Column address selector) has already selected the row address and usually D-RAMs do not use the A0 signal as row address directly, the buffer of U40 is made enable, and only the period of refreshment, the buffer of U40 converts the A0 signal to the MA6 signal.

The procedure mentioned above is a one cycle refreshment operation. The DMAC increments and counts up the row address with every 15 micro seconds of interruption from the PIT.

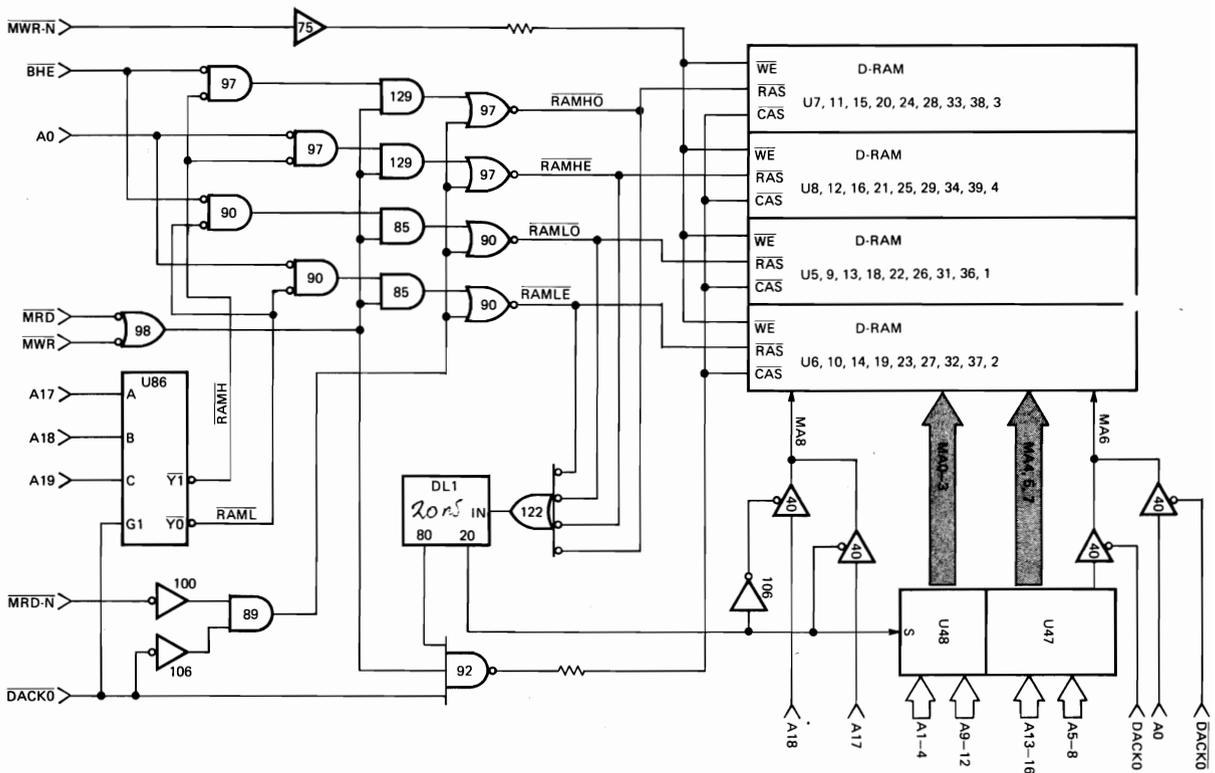


Figure 6-9

• Parity Checking

RAMs have 1 bit of parity bits corresponding to every one byte of even addresses and odd addresses. Parity bits are generated by U30 for even addresses and by U41 for odd addresses. These ICs generate an even parity and odd parity according to 9-bit data input to the A through I terminals. When writing data into RAM, their I terminals become LOW with the MRD signal output from U77, and then U30 and U41 input data (MD0 through MD7 for even addresses, MD8 through MD15 for odd addresses) to their A through H terminals, and finally get respective even parities (MDEIP, MDOIP) before writing data to RAMs.

When reading, U30 and U41 input data (MD0 through MD7 for odd addresses and MD8 through MD15 for even addresses) read from RAMs into their A through H terminals, and input the parity bit (MDEOP for even address and MDOOP for odd address) into I terminal to ensure that read data is valid.

If any one bit is missing in reading, Sigma-ODD terminal of U30 or U41 becomes HIGH. This signal makes to send Non Maskable Interrupt signal to the CPU at the rising edge of the $\overline{\text{MRD-N}}$ signal after it has been ANDed with the A0 or $\overline{\text{BHE}}$ signal.

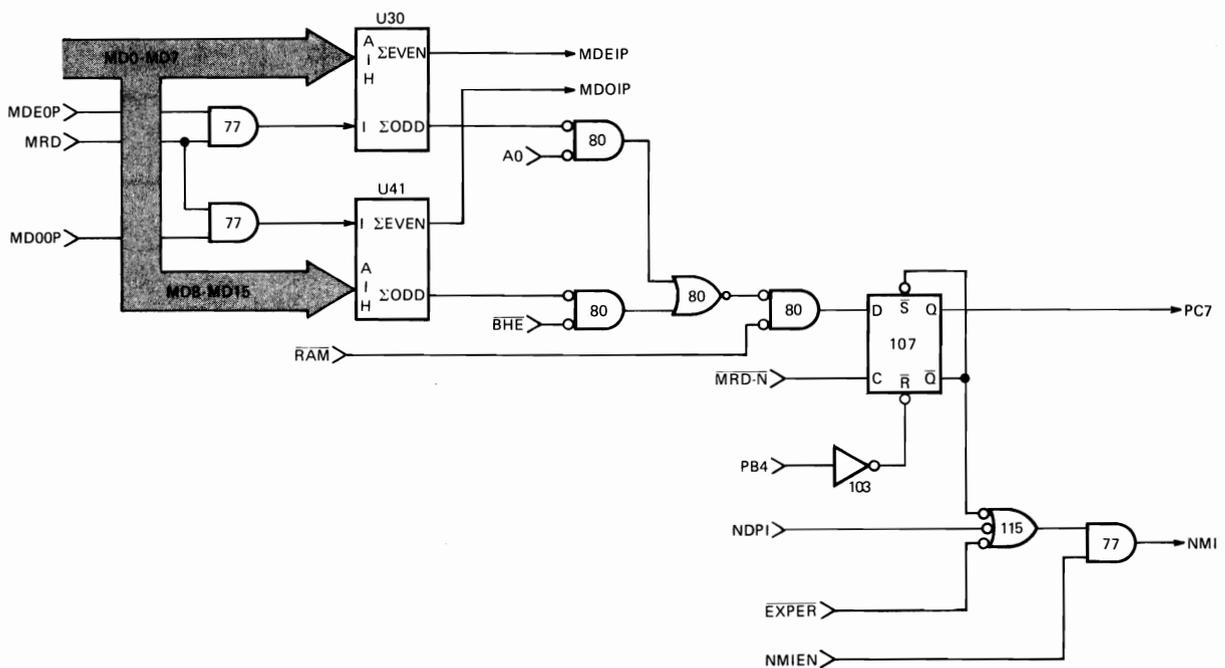


Figure 6-10

VI-2-6. I/O Map and I/O Address Decoding Circuit

Figure 6-11 shows the I/O address decoding circuit. This circuit generates the chip enable signals for LSIs and registers mounted on the main P.C.B.

The decoder U51 generates the chip enable signal for the I/O devices existing on the I/O addresses 000 to 0FF, and U117 generates the chip enable signal for the I/O devices existing on the I/O addresses 360 to 3FF.

Table 6-2 shows the schema of I/O map.

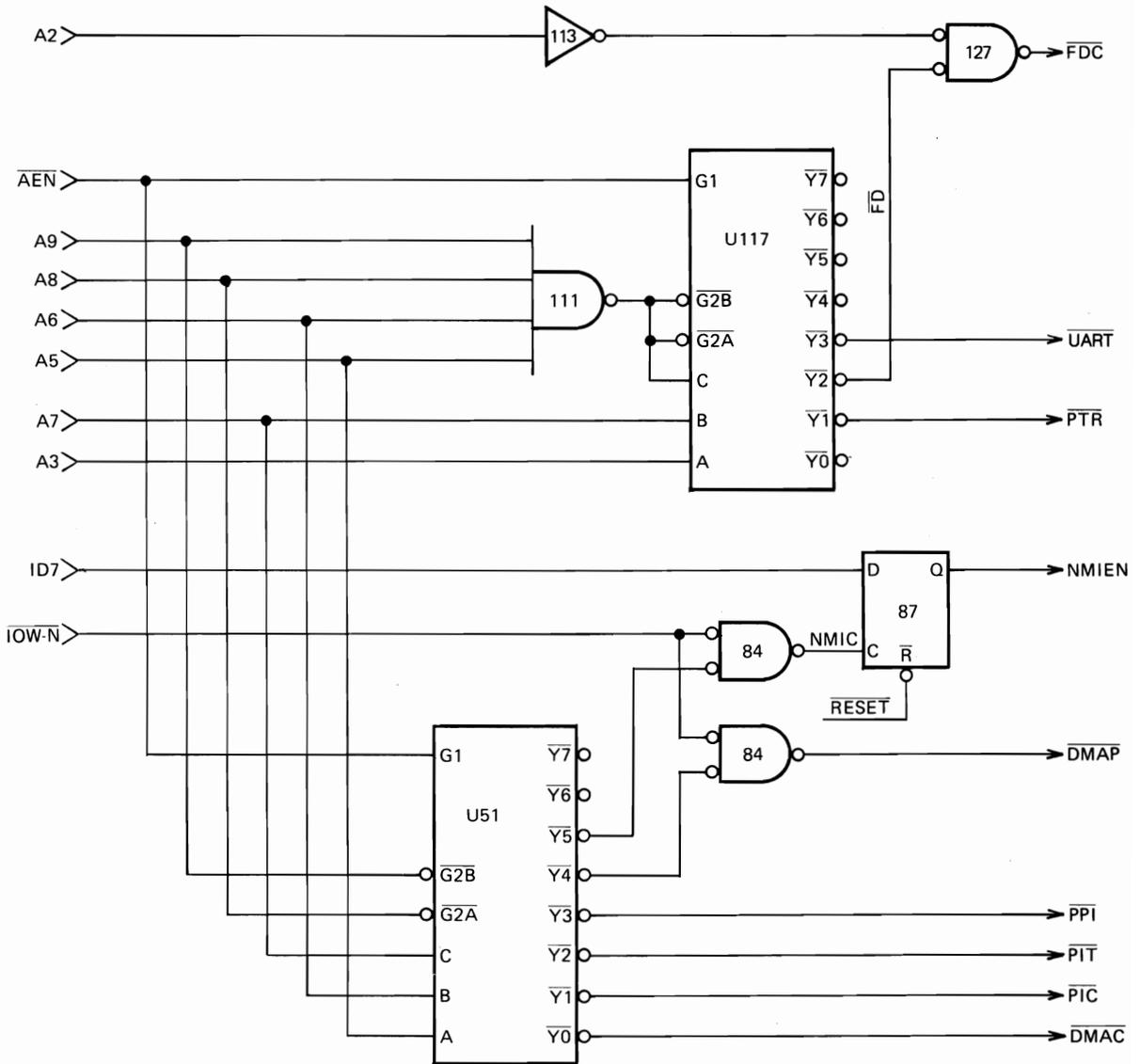


Figure 6-11

I/O Address		WRITE	READ
0000	DMAC	CH0 base, current address	CH0 current address
0001		CH0 base, current word count	CH0 current word count
0002		CH1 base, current address	CH1 current address
0003		CH1 base, current word count	CH1 current word count
0004		CH2 base, current address	CH2 current address
0005		CH2 base, current word address	CH2 current word count
0006		CH3 base, current address	CH3 current address
0007		CH3 base, current word address	CH3 current word count
0008		Common register	Status
0009		Request register	×
000A		Single mask register bit	×
000B		Mode register	×
000C		Clear byte pointer flip-flop	×
000D		Master clear	Temporary register
000E		Clear mask register	×
000F		All mask register bit	×
0020	PIC	ICW1, ICW2, OCW3	IRR, ISR/interrupt level
0021		ICW2, ICW3, ICW4, OCW1	IMR
0040	PIT	Counter #0 load	Counter #0 read
0041		Counter #1 load	Counter #1 read
0042		Counter #2 load	Counter #2 read
0043		Control word	×
0060	PPI	Port A	Port A
0061		Port B	Port B
0062		Port C	Port C
0063		Control word	×

I/O Address		WRITE	READ
0080	DMA Reg.	×	×
0081		DMA CH2 upper address for FDD	DMA CH2 upper address for FDD
0082		DMA CH3 upper address	DMA CH3 upper address
0083		DMA CH1 upper address	DMA CH1 upper address
00A0 ~ 00AF	NMI Reg.	NMI mask register	×
0378	PRINTER	Printer data	Echo data
0379			Printer status
037A		Printer output control	Printer status
03B4	Mono Board	68B45 index register	×
03B5		68B45 Data register	68B45 data register
03B8		CRT control port	×
03BA		×	CRT status port
03D4	Color Board	68B45 index register	×
03D5		68B45 data register	68B45 data register
03D8		Mode control register	×
03D9		Color select register	×
03DA		×	Status resister
03DB		Reset light pen latch	×
03DC		Set light pen latch	×
03F0	FDC	FDD control register	×
03F4		Command register	Status register
03F5		Data register	Data register
03F8	UART	Transmitter holding register	Receiver buffer
03F9		Interrupt enable	
03FA			Interrupt
03FB		Line control	
03FC		Modem control	
03FD			Line status
03FE			Modem status
03FF		×	×

Table 6-2

VI-2-7. System Bus

The CPU transfers data between I/O devices and memory through three buses. First of them is the address bus and it defines I/O or memory addresses. The data bus sends data through it. The command bus determines functions of address and data buses.

As previously mentioned, basically the A-200 has the 16-bit bus constructions, however, it can access to a memory board or optional board designed for the IBM-PC that are constructed with 8-bit bus.

Figure 6-12 shows the bus construction.

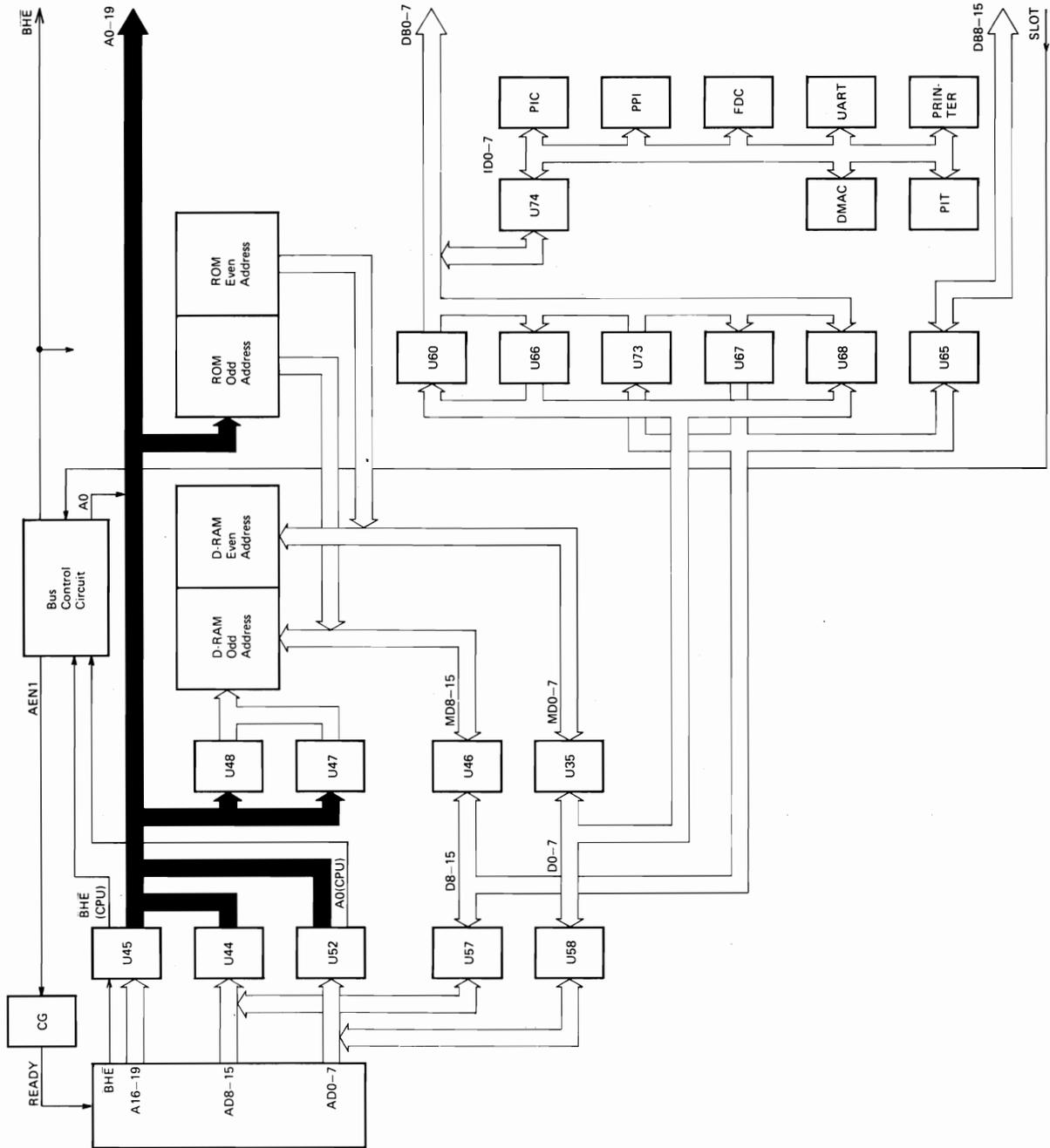


Figure 6-12

The pins AD0 through AD15 of the CPU are the time multiplexed address and data bus. U52 and U44 separates the contents of the address bus using the ALE signal that is obtained by encoding the status signals $\overline{S0}$ through $\overline{S2}$ from the CPU at the BCU.

Similarly, signals A16 through A19 are generated from A16/S3 through A19/S6 signals respectively with U45 by using the ALE signal.

Among above 20-address signals, only lowest bit A0 (CPU) signal is used with the \overline{BHE} (CPU) signal to determine whether lower 8 bits (D0 — D7) or upper 8 bits (D8 — D15) are accessed. If an optional board which has 8-bit bus construction is used, this A0 (CPU) signal is also used by the bus control circuit to generate odd addresses when it executes a word transfer (2 bytes) beginning from even addresses. That is, the bus control circuit makes the lowest bit A0 to LOW first, and then data in even addresses are transferred to the lower 8 bits in the data bus, and makes the CPU to WAIT state. Finally, the A0 becomes HIGH and then data in odd addresses are transferred to the upper 8 bits in the data bus.

Thus, the lowest address line bit A0(CPU) signal and \overline{BHE} (CPU) signal that gives a permission to use the upper 8 bits of the data bus are not sent to the memory or I/O devices directly.

They are converted to the A0 and \overline{BHE} signals respectively according to current transfer modes, and then they are sent to memory or I/O devices.

AD0 through AD15 are connected to the data bus through bi-directional buffers U57 and U58. The chip enable terminals and the direction terminals of these ICs are connected to the DEN and the T/R terminals of the BCU. Therefore, when the CPU assigns the A0 through A15 as data bus, these buffers become enable.

When accessing on-board RAM or ROM, data bus is connected to these memories through U35 and U46. The reason of this is as follows; since RAMs and ROMs mounted on the main board have 16-bit bus construction, one byte data in even address is transferred to D0 through D7, one byte data in odd address is transferred to D8 through D15 respectively, data begins from even address is transferred to D0 through D7 and data begins from odd address is transferred to D8 through D15 when in one word (2 bytes) transfer mode. If RAMs or V-RAMs mounted on an optional board have 16-bit data bus construction, they are connected to the data bus through U68 and U65.

Another two latches and buffers are effective only for memory or I/O devices having 8-bit data bus construction. Usually, one of two latches works in read operation and one of two buffers works in write operation during the CPU cycle. The combination for using these gates depends on four factors — accessing from the CPU, accessing from the DMAC, even address and odd address. Detail of their combination are indicated in Table 6-3.

The command bus consists of \overline{MRD} , \overline{MWR} , \overline{IOR} , \overline{IOW} , DEN, T/R, and ALE signals. The BCU generates these signals using the status signals $\overline{S0}$ through $\overline{S3}$ from the CPU and \overline{AEN} , CEN and \overline{INTA} signals from the I/O devices. These signals are used by the CPU when it accesses memory or I/O. However, when the DMAC accesses memory or I/O without CPU's intervention, it generates peculiar \overline{MRD} , \overline{MWR} , \overline{IOR} and \overline{IOW} signals.

Table 6-4 describes about the signals in command bus.

	CPU cycle	DMA cycle
Write buffer (D0 — D7) U60	* Writes to even addresses. * Inhibited when accessing a 16-bit board.	* Reads even addresses of main memory.
Read latch (D0 — D7) U66	* I/O read, INTA cycle * Inhibited when accessing main memory and/or 16-bit board memory	* Writes to main memory and/or 16-bit board memory.
Write buffer (D8 — D15) U73	* Writes to odd addresses. * Inhibited when accessing 16-bit board.	* Reads odd addresses of main memory and/or 16-bit board memory.
Read latch (D8 — D15) U67	* I/O read * Inhibited when accessing main memory and/or 16-bit board memory.	* Writes to main memory and/or 16-bit board memory.
Data buffer (D0 — D7) U68	* Accesses even addresses of 16-bit board.	* Inhibited
Data buffer (D8 — D15) U65	* Accesses odd addresses of 16-bit board.	* Reads/writes main memory and/or 16-bit board memory.

Table 6-3

Signal	Description
$\overline{\text{MRD}}$	Memory read command
$\overline{\text{MWR}}$	Memory write command
$\overline{\text{IOR}}$	I/O read command
$\overline{\text{IOW}}$	I/O write command
$\overline{\text{DEN}}$	Data enable signal for data transceivers
T/R	Direction signal for Data transceivers when "H", the transceiver becomes write mode, when "L", becomes read mode.
ALE	Strobe signal for address latches. The down edge of this signal latches address signals from the CPU.

Table 6-4

VI-2-8. DMAC

The DMAC performs two important operations. One is a data transfer between memory and I/O devices and the other is refreshment for D-RAMs. However, the relationship between these two operations and the CPU is basically identical.

Figure 6-13 shows a concept for the DMA operation.

As for the A-200, the DMA operation is performed in the cycle steal mode and so, an insertion of the wait cycle is done by using the READY signal.

The DREQ signal from the I/O notifies the DMAC of a DMA request. Then the DMAC also notifies the CPU of that DMA request by making the \overline{HRQ} signal LOW.

For the DMAC to judge whether an instruction cycle has been completed or not, this \overline{HRQ} signal becomes to the DMAGO signal at U79 by being ANDed with $\overline{S0}$, $\overline{S1}$, $\overline{S2}$ and \overline{LOCK} signals. This DMAGO signal is latched by U109 at the falling edge of the CLK signal and becomes the HOLDA signal.

The HOLDA signal tells the DMAC that the CPU will insert TW signal between T3 and T4.

While, a signal delayed for a half clock cycle at U108 becomes the AEN signal, and an inverted signal of it — \overline{AEN} is sent to the CEN terminal of the BCU and finally, it makes the BCU inactive.

The AEN signal is then delayed for one clock cycle at U108 and becomes LOW level RDY1 signal.

This signal makes the READY terminal of the CPU to LOW. The CPU keeps inserting TW signal between T3 and T4 during LOW level of that terminal.

The DMAC performs data transferring between the I/O and memory while the CPU keeps inserting TW signals.

In addition, since an address control of the DMAC requires 16-bit bus, U78 makes up for want of 4 bits.

Figure 6-14 and 6-15 show the timing chart for the DMA operation and one for refreshment for D-RAMs respectively.

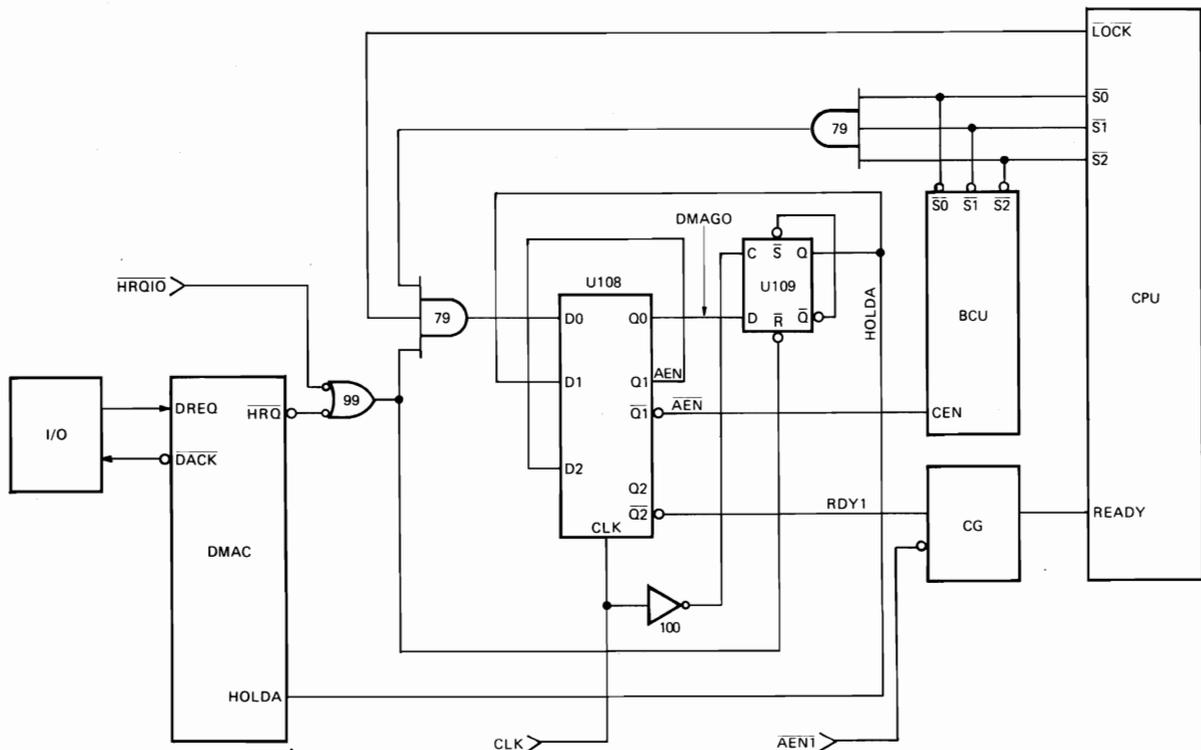


Figure 6-13

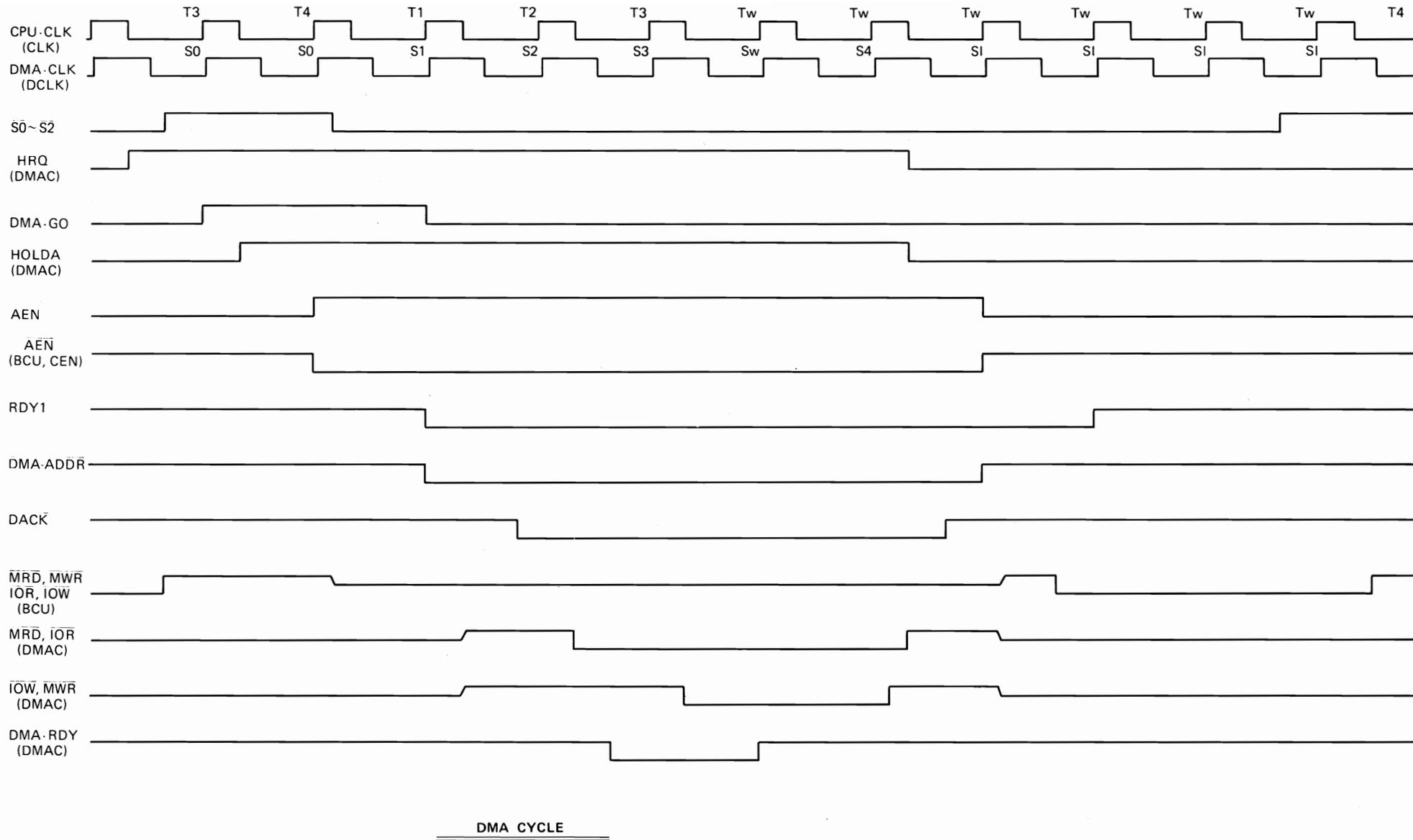
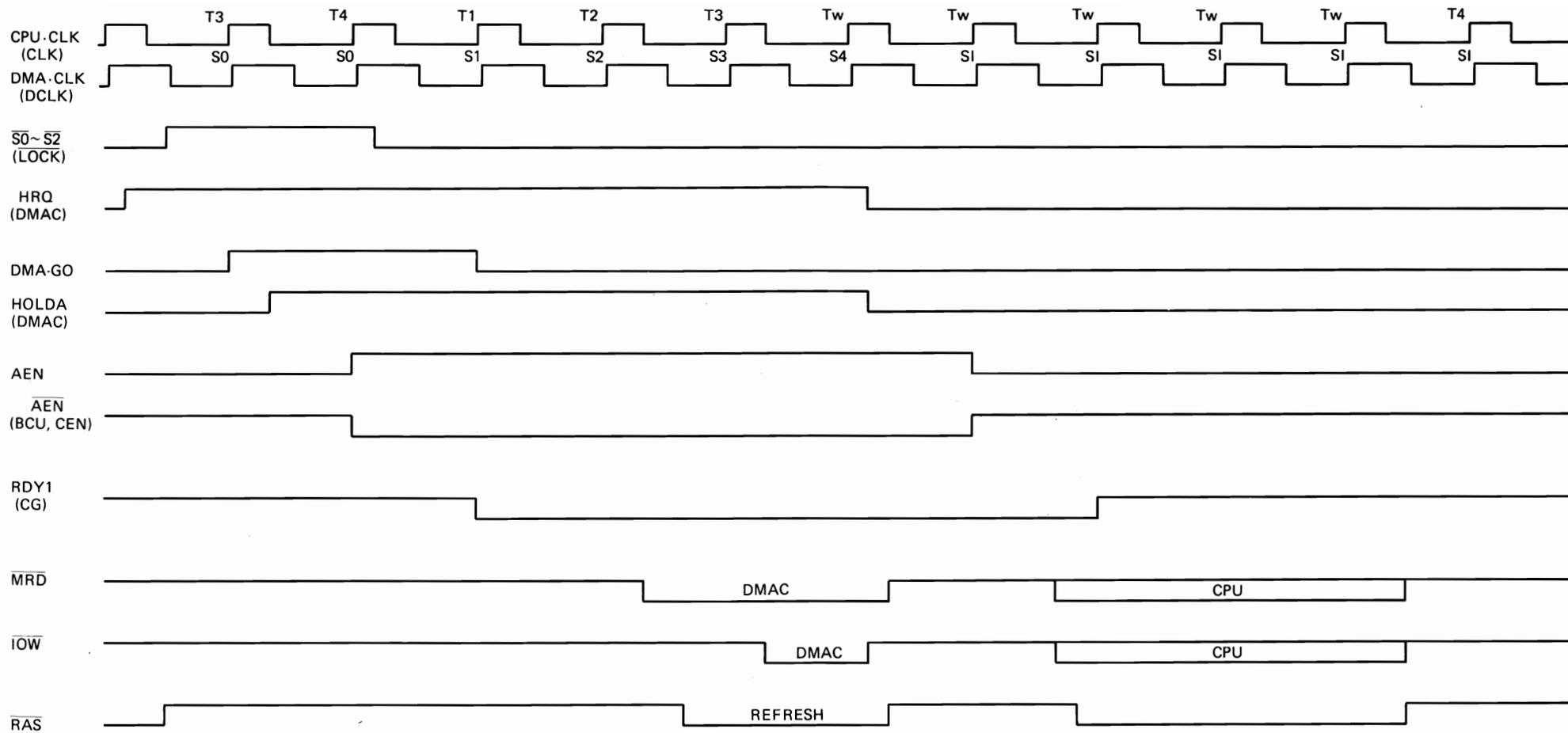


Figure 6-14



DMA REFRESH

Figure 6-15

VI-2-9. Printer Interface Circuit

Figure 6-16 shows the printer interface circuit. This circuit consists of two output latches (U42 and U49), three input buffers (U138, U139 and U64) and a decoder circuit which selects the functions of these latches and buffers.

When the CPU assigns addresses 378 through 37FH as I/O addresses, a LOW level $\overline{\text{PTR}}$ signal is sent to U110. U110 then makes each latch and buffer enable by decoding A0, A1, $\overline{\text{IOW-N}}$ and $\overline{\text{IOR-N}}$ signals.

Table 6-5 shows the definition for data bus at each I/O address. Figure 6-17 shows the timing chart at printing.

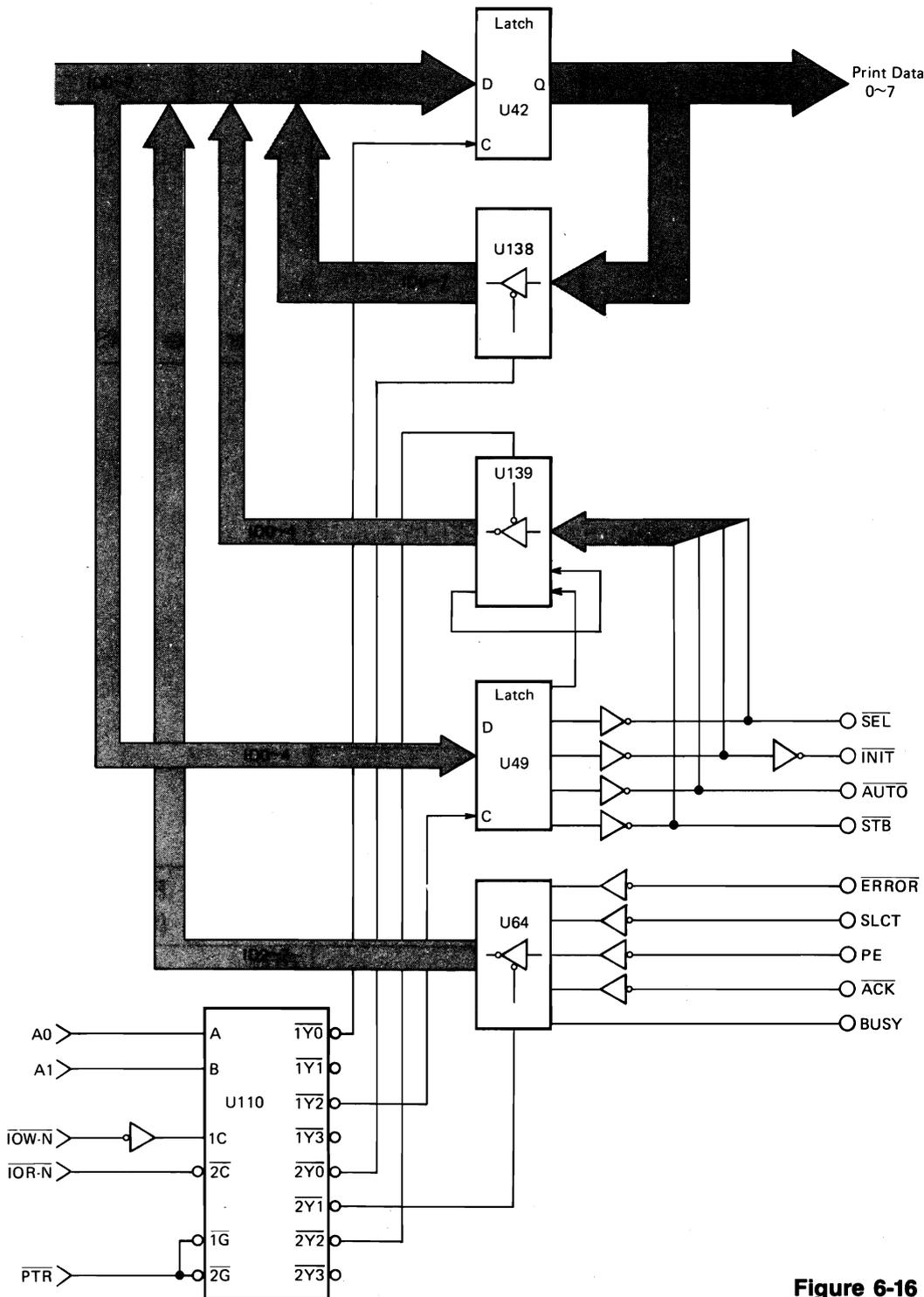


Figure 6-16

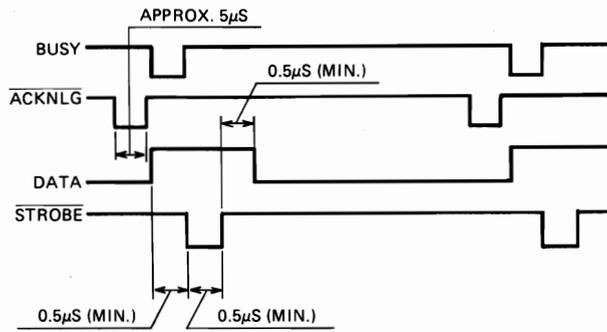


Figure 6-17

I/O Address	Data	WRITE (U42)	READ (U138)
378	D0	Printer Data 0 LSB	Printer Data 0 LSB
	D1		
	D2		
	D3		
	D4		
	D5		
	D6		
	D7		

I/O Address	Data	READ (U64)
379	D0	—
	D1	—
	D2	—
	D3	$\overline{\text{Error}}$
	D4	Select
	D5	Paper Empty
	D6	$\overline{\text{Acknowledge}}$
	D7	Busy

Table 6-5

I/O Address	Data	WRITE (U49)	READ (U139)
37A	D0	$\overline{\text{STB}}$	$\overline{\text{STB}}$
	D1	$\overline{\text{AUTO FEED}}$	$\overline{\text{AUTO}}$
	D2	$\overline{\text{INITIALIZE}}$	$\overline{\text{INIT}}$
	D3	$\overline{\text{SELECT}}$	$\overline{\text{SEL}}$
	D4	—	—
	D5	—	—
	D6	—	—
	D7	—	—

VI-2-10. RS-232C Interface Circuit

This circuit consists of the transmitter U50, receivers U43 and U55 and the UART (8250), the heart of this circuit.

U50 converts TTL compatible signals from the UART to $-12V$ to $+12V$ signals conforming to the EIA standard, and output them.

U43 and U55 convert EIA level reception signal to TTL level, and send them to the UART. The functional configuration of the UART is programmed by the software via the data bus.

The UART performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud generator. Also included in the UART is a complete MODEM control capability, and a processor-interrupt system that minimize the computing time required to handle the communications link.

The interrupt signal is sent to IR4 terminal of the PIC through the bit4 or the DIP switch S2.

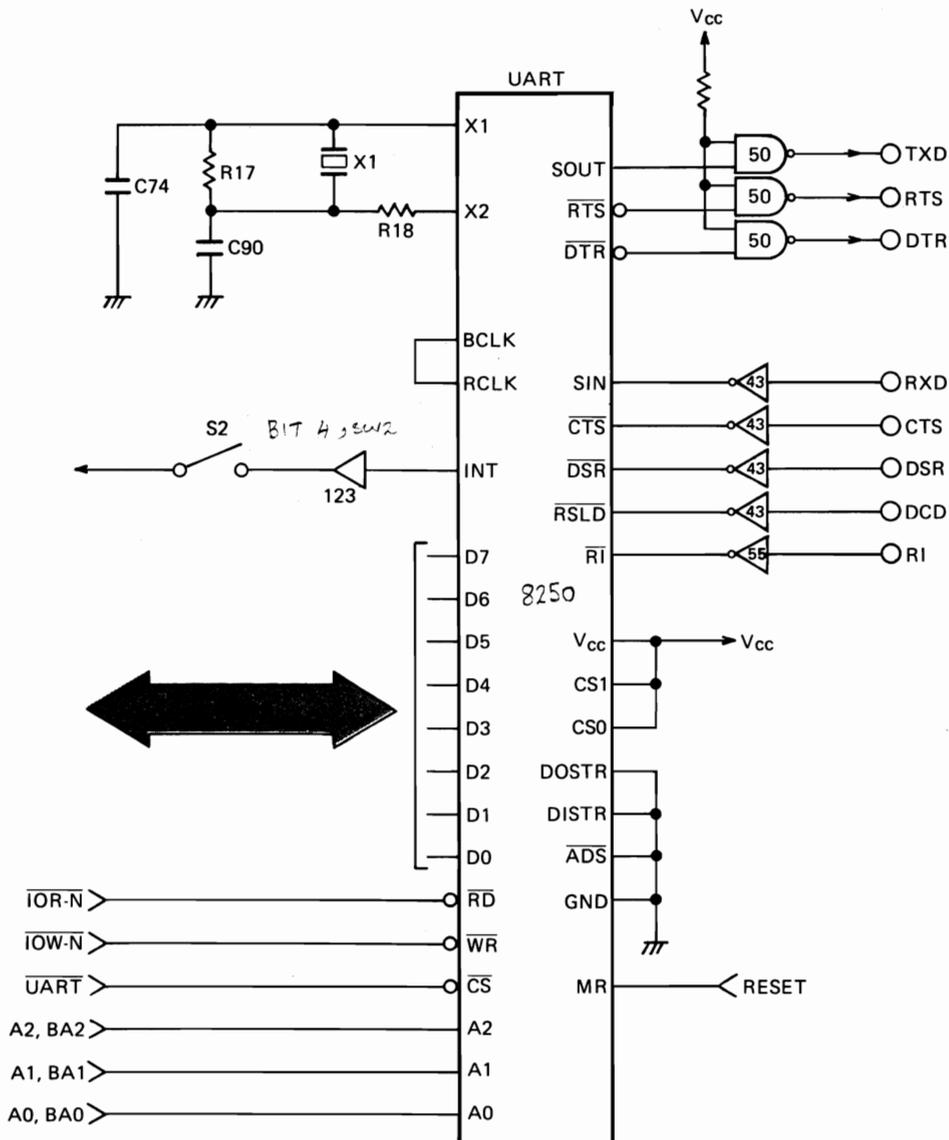


Figure 6-18

UART has the following significant features:

- * Full double buffering eliminates need for precise synchronization.
- * Independently controlled transmit, receive, line status, and data set interrupts.
- * Programmable baud generator allows division of any input clock by 1 to $(2^{16}-1)$ and generates the internal $16 \times$ clock.
- * Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data stream.
- * Line break generation and detection.
- * Internal diagnostic capabilities:
 - Loopback controls for communications link fault isolation.
 - Break, parity, overrun, framing error simulation.
- * Full prioritized interrupt system controls.
- * MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD).
- * Fully programmable serial-interface characteristics:
 - 5; 6; 7; or 8-bit characters
 - Even, odd, or no-parity bit generation and detection.
 - 1; 1-1/2; or 2-stop bit generation
 - Baud generation (DC to 56k baud).
- * False start bit detection.
- * Complete status reporting capabilities.

When the CPU assigns one of addresses 3F8 through 3FFH as I/O address, the LOW level UART signal from the I/O address decoding circuit is sent to the UART. The UART then selects the internal register to be connected to the data bus according to the status of A0 through A2 terminal and \overline{RD} and \overline{WR} terminal, and the status of DLAB (Divisor Latch Access Bit).

-DLAB is bit7 of the line control register.

Table 6-6 shows the status of registers indicated by each I/O address.

I/O Address	A2	A1	A0	\overline{RD}	\overline{WR}	DLAB	
3F8	L	L	L	L	H	X	Receive Buffer
3F8	L	L	L	H	L	X	Transmit Buffer
3F8	L	L	L	*	*	1	Divisor Latch LSB
3F9	L	L	H	*	*	1	Divisor Latch MSB
3F9	L	L	H	*	*	0	Interrupt Enable Register
3FA	L	H	L	*	*	X	Interrupt Identification Register
3FB	L	H	H	*	*	X	Line Control Register
3FC	H	L	L	*	*	X	MODEM Control Register
3FD	H	L	H	*	*	X	Line Status Register
3FE	H	H	L	*	*	X	MODEM Status Register

*: \overline{RD} becomes LOW when read operation.

\overline{WR} becomes LOW when write operation.

X: Don't care.

Table 6-6

VI-2-11. Timer and Speaker Driver Circuit

Figure 6-19 shows the timer and speaker driver circuit. Mainly, this circuit has the following functional features.

- * Generates an interruption signal when the predetermined timer becomes active.
- * Requests the DMAC to refresh D-RAMs at every 15 micro seconds.
- * Determines frequency of a signal to be sent to the speaker.

Above operations are performed based on a clock signal which is obtained by dividing the frequency of the PCLK signal (2.39MHz) from the CG into a half at U107.

The PIT has three sets of 16-bit counter, and they have independent output terminals OUT0, OUT1 and OUT2 respectively.

The OUT0 terminal sends an interruption signal to the CPU through the PIC when the predetermined timer counting has been completed.

The OUT1 terminal outputs a refresh request signal to the DMAC at every 15 micro seconds. This signal is latched by U87 and is reset by an acknowledgement signal ($\overline{DACK0}$) sent from the DMAC.

The OUT2 terminal generates an audio frequency signal for the speaker according to requirements of the software. This signal is Nanded with the PB1 signal sent from the PPI and then drives the transistor Q3 to sound the speaker.

Table 6-7 shows data loadings and reading for every counter.

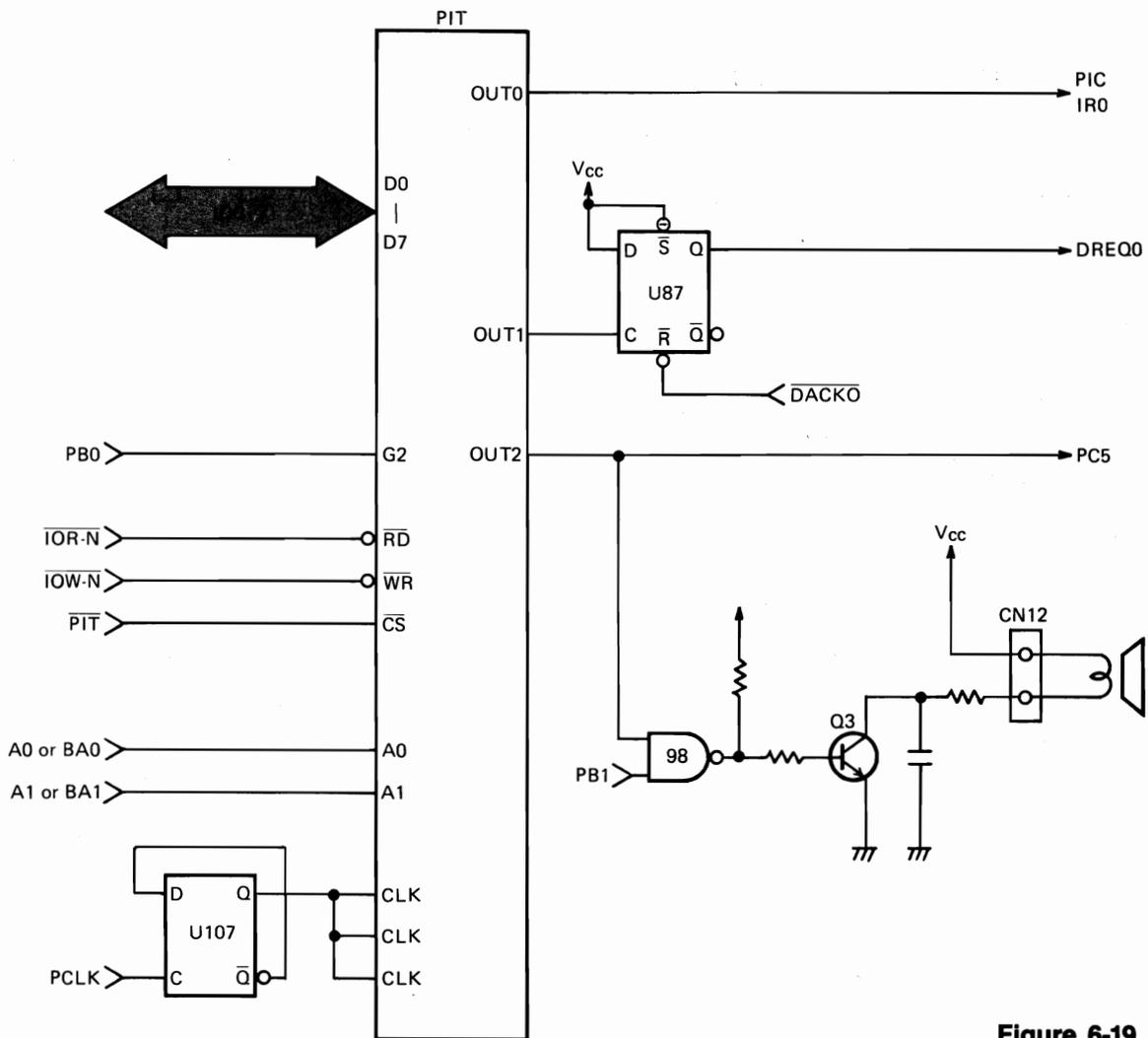


Figure 6-19

I/O Address	A1	A0	\overline{RD}	\overline{WR}	
0040	L	L	L	H	Read Counter No.0
0040	L	L	H	L	Load Counter No.0
0041	L	H	L	H	Read Counter No.1
0041	L	H	H	L	Load Counter No.1
0042	H	L	L	H	Read Counter No.2
0042	H	L	H	L	Load Counter No.2
0043	H	H	L	H	No-operation (3-state)
0043	H	H	H	L	Write Mode Word

Table 6-7

VI-2-12. Keyboard Interface

The keyboard interface converts serial data comes from the keyboard unit to parallel data. Another role of this circuit is to notify the soft reset status to the one chip microprocessor (8048) mounted on the internal board of the keyboard unit.

Above functions are performed by using two bi-directional interface signals, KDATA and KCLK. Before sending data, the keyboard unit confirms that neither KCLK signal nor KDATA signal is HIGH level. If so, it sends data as shown in Figure 6-20.

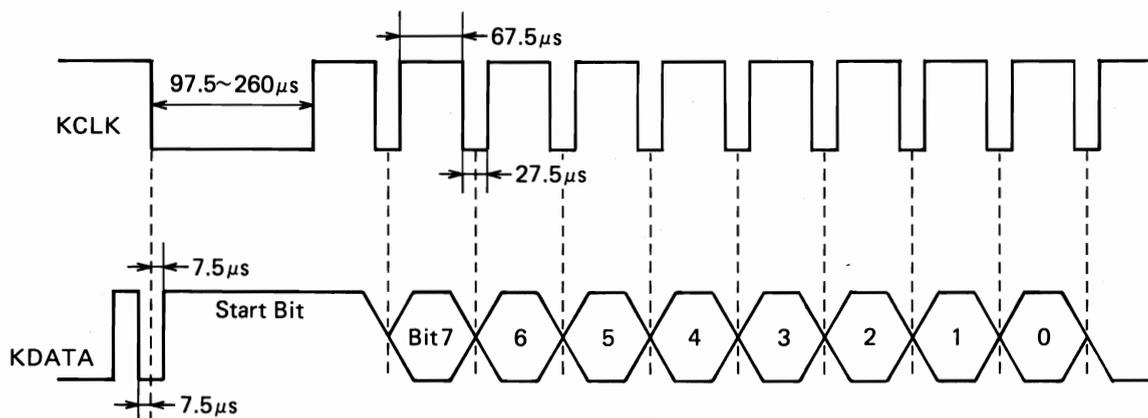


Figure 6-20

First data to be sent to this interface is the start bit (HIGH level) which denotes that an 8-bit data will follow it. This data will then be sent to the \overline{SL} (Shift Left) terminal of the shift register U94. As for the KCLK signal, it is not only converted through two stages of flip-flop but also synchronized with the clock signal inside the main P.C.B. (PCLK).

In this case, since a cycle of the KCLK is approximately 100 micro seconds while a cycle of the PCLK is approximately 400 nano seconds, a delay of the KCLK signal is not an important factor in receiving key data. The inverted KCLK signal is input to the CLK terminal of U49, then shifts the 8-bit data followed by the start bit sequentially at every falling edge of the KCLK signal. When the eighth falling edge comes, U94 then outputs HIGH level start bit from its QA terminal. Thus at the ninth falling down edge of the KCLK signal, U94 sends an interrupt signal to the CPU from U109 through the PIC indicating that one byte of key data is now ready for use. At the same time, the \overline{Q} terminal of U109 makes U123 connected to the KDATA line enable and then forces the KDATA line to become LOW level.

Before sending data, the keyboard unit always checks the logical level of the KDATA line. Therefore, it does not send the next key data unless the PB7 signal of the CPU becomes HIGH after the CPU receives the interruption signal and processes an 8-bit parallel data in the shift register.

Sending the soft reset signal to the keyboard unit is done by keeping the PB6 signal LOW for more than 20 milli seconds.

By doing so, the KCLK line is forced to become LOW by U123. When the one chip microprocessor in the keyboard unit detects this LOW level signal, it performs the soft reset.

When the soft reset signal is sent to the keyboard unit, the microprocessor in the keyboard will begin to execute the self-diagnostic program, and then sends 1-byte return code to the keyboard interface.

On the main P.C.B., the RESET signal is connected to the keyboard connector through U100 and U123, however, this signal is not used by the keyboard unit.

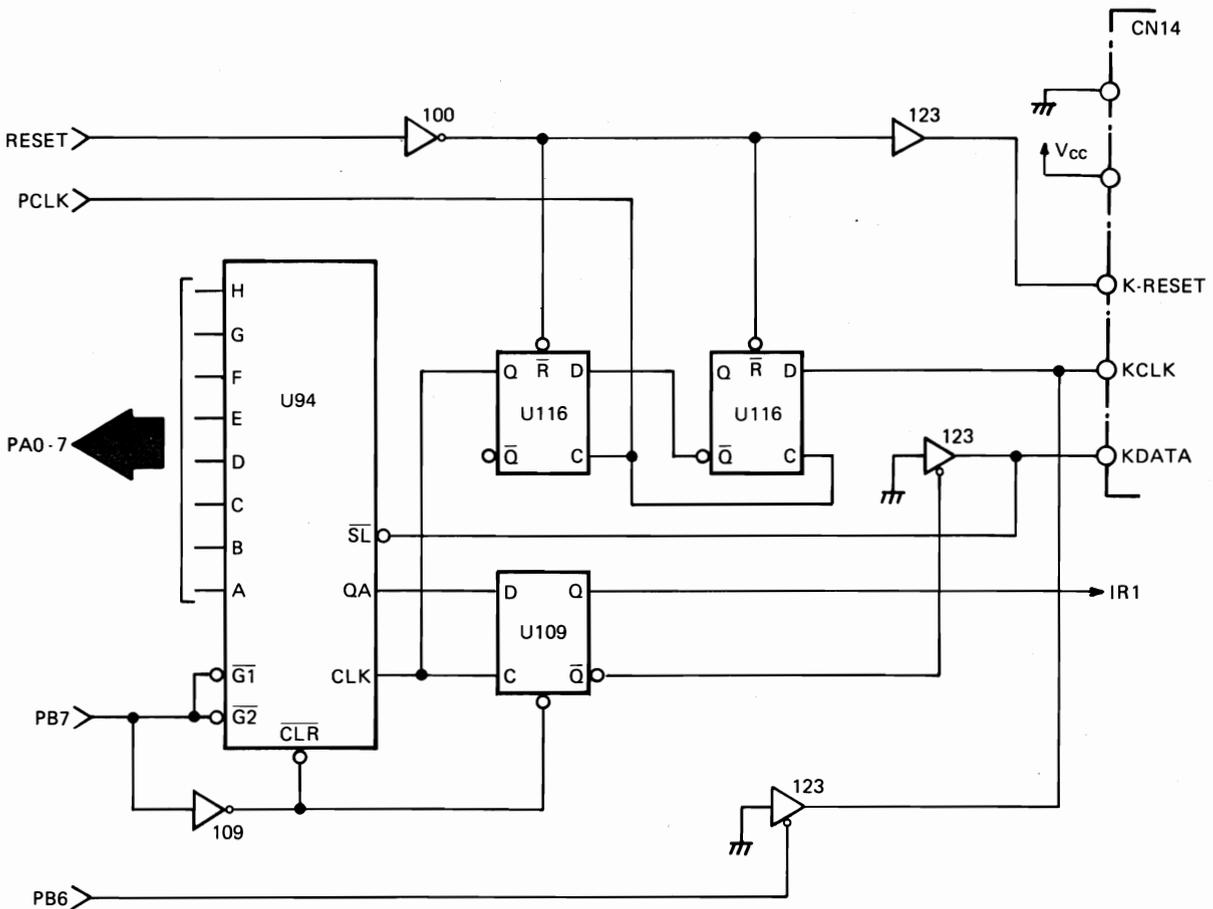


Figure 6-21

VI-2-13. PPI

The A-200 employs the 8255 as the PPI. This LSI is used in MODE0. In this mode, the port A, port B, upper 4 bits of port C and lower 4 bits of port C can be assigned as either of input ports or output ports independently.

In the A-200, the port A and upper and lower bits of the port C are used as inputs, and the port B as outputs.

Table 6-8 shows the port assignments.

I/O Address	Terminal	I/O	Description	
60	PA0	I	PB7=L	PB7=H IPL 5-1/4" disk drive* 8087 installed System Memory Size System Memory Size Display Type Display Type Number of disk drive Number of disk drive**
	PA1	I	Key Data (LSB)	
	PA2	I	Key Data (LSB)	
	PA3	I	Key Data (LSB)	
	PA4	I	Key Data (LSB)	
	PA5	I	Key Data (LSB)	
	PA6	I	Key Data (LSB)	
	PA7	I	Key Data (LSB)	
61	PB0	O	PIT G2 terminal	
	PB1	O	Speaker data	
	PB2	O	Not used	
	PB3	O	Not used	
	PB4	O	System Memory Parity Enable	
	PB5	O	Optional Memory Parity Enable	
	PB6	O	Soft Reset for Keyboard Unit	
	PB7	O	Enable K/B data or DIP Switch Status	
62	PC0	I	Optional RAM Size	
	PC1	I	Optional RAM Size	
	PC2	I	Optional RAM Size	
	PC3	I	Optional RAM Size	
	PC4	I	Not used	
	PC5	I	PIT OUT 2 terminal	
	PC6	I	Optional Memory Parity Check	
	PC7	I	System Memory Parity Check	

* Pull up to Vcc ** Pull down to ground

Table 6-8

PA0 through PA7 terminals of the port A determines whether it selects a shift register U94 or the status of the DIP switch, depending on the logical level of the PB7 terminal. When this terminal is LOW, it selects the former, and when HIGH, the later. For more detailed information concerning the DIP switches, refer to "Summary of DIP Switch Setting" in Part IV of this manual.

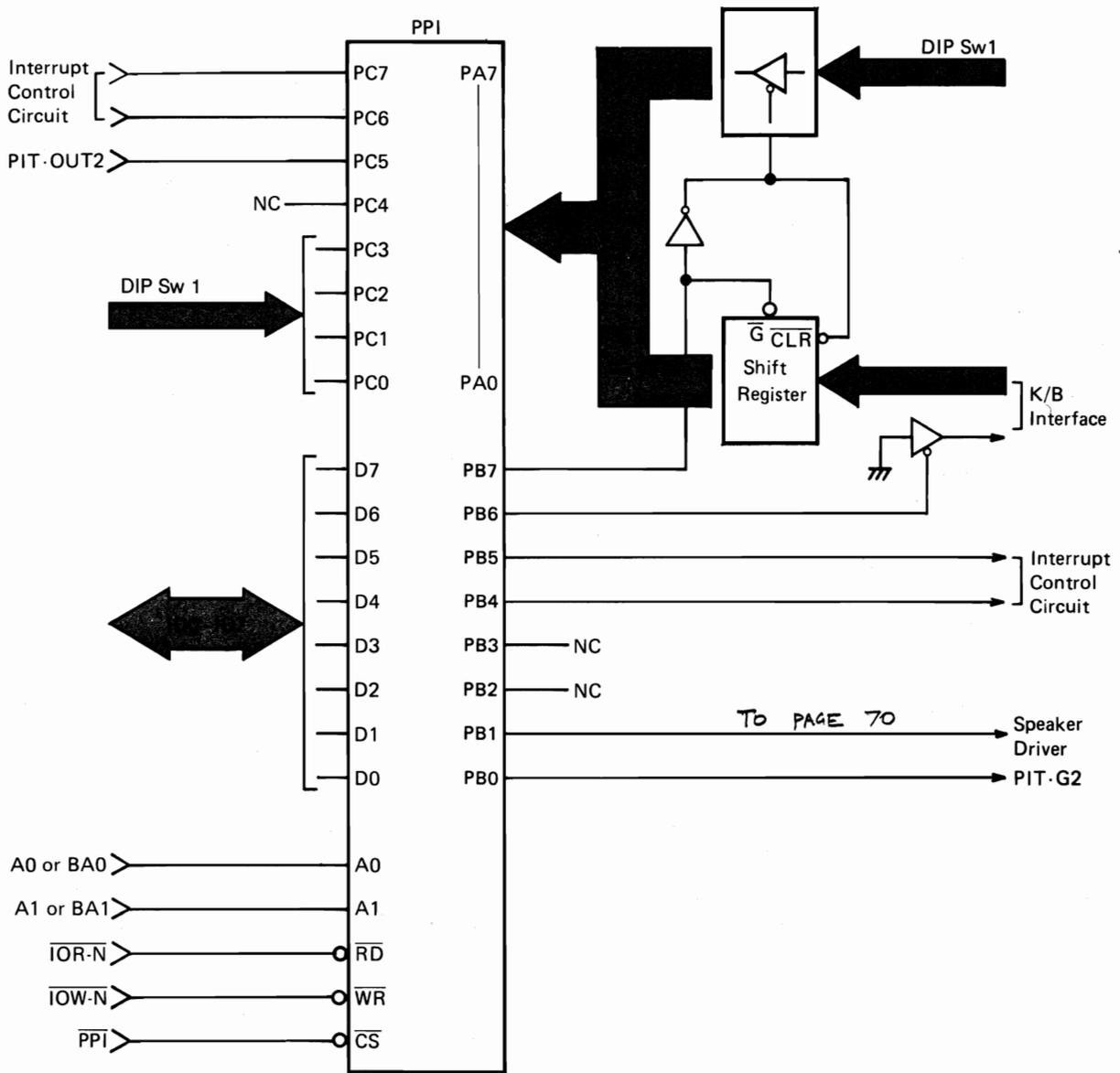


Figure 6-22

VI-2-14. FDD Interface Circuit

For simplicity we have divided this paragraph into the following five sections:

- * FDD Control Register
- * Clock Generator Circuit
- * FDC
- * Pre-Compensation Circuit
- * Data Separation Circuit

• FDD Control Register

This register selects the FDD unit A or B, resets the FDC and defines whether it permits an interruption of the FDC or DMA request or not. It consists of 4-bit flip-flop circuits. Descriptions for each bit are mentioned in Table 6-9.

I/O Address	Bit	Description
3F0	2	FDC is reset when this bit is LOW.
	3	H level of this bit allows FDC interruption and DMA request.
	4	L level of this bit selects Drive A
	5	L level of this bit selects Drive B

Table 6-9

Figure 6-23 shows operations of the FDD Control Register.

Data transfer between the FDD and memory is made through the DMAC and FDC.

The FDC sends the DREQ signal to the DMAC when data transfer to/from the FDD becomes enable. This signal is delayed for the time equivalent to four 2MHz clock cycles (2 micro seconds) and then sent to the DREQ2 terminal of the DMAC after it is ANDed with the bit 3 of the FDD control register.

When the DMAC receives the DMA request, it makes the CPU wait, and then sends the $\overline{DACK2}$ signal to the FDC to begin the DMA transferring. When one block of data transfer is completed, the FDC sends an interruption signal through the IRQ6 terminal of the PIC.

• Clock Generator Circuit

This circuit emits 16MHz, 8MHz and 2MHz clock signals used for the FDD interface circuit. The 16MHz-clock is used as a fundamental clock for U104 (SED9420C0B) and as a clock input for the counter IC, U95.

Further, U104 emits 4MHz of clock signal by dividing the fundamental clock by four and then supplies it to the FDC.

U95 generates 8MHz and 2MHz clock signals by dividing it by two and eight.

• FDC

This circuit employs the IC μ PD765AC. Followings are descriptions for each pin of this IC.

Pin Name	I/O	Description
ϕ	I	Input for 4MHz clock.
RESET	I	Makes the FDC idle and makes drive interface output other than PS0, PS1 and WDATA LOW. And makes INT and DRQ outputs LOW.
\overline{CS}	I	Makes RD, WR signals effective.
DB7 — DB0	I/O	Bi-directional, 3-state data bus
\overline{WR}	I	Control signal for writing data to the FDC through the data bus.
\overline{RD}	I	Control signal for reading data from the FDC through the data bus.
INT	O	This signal indicates that the FDC requires accessing and is output at every one byte in NON DMA mode, and at the end of command in DMA mode.
A0	I	Selects status register or data register in the FDC accessed through the data bus.
DRQ	O	Requests data transfer between the FDC and memory in DMA mode.
\overline{DACK}	I	This signal indicates that the DMA cycle is given. This acts similar to the CS signal in the DMA cycle.
MFM	O	Determines an operation mode of the VFO circuit. MFM mode when HIGH, FM mode, LOW.
SYNC	O	Determines an operation mode of the VFO circuit. Permits reading when HIGH, inhibits, LOW.
RW/SEEK	O	Selects the functions of a signal used as both read/write and seek. RW when LOW, SEEK when HIGH.
SIDE	O	Select head 0 or head 1 when dual-sided drive is used. LOW for head 0, HIGH for head 1.
LCT/DIR	O	When RW/SEEK signal is in RW mode, this becomes LCT and indicates that the W/R head of the drive is selecting more than 43 cylinders. When RW/SEEK is in SEEK, this becomes DIR and determines a direction for seek. LOW for inner direction, HIGH for outer.
FLTR/STEP	O	When RW/SEEK is in RW, this becomes FLTR and resets FAULT status in the drive. When RW/SEEK is SEEK, becomes STEP and send a step signal for seek.
READY	I	Indicates that the drive is ready.
WPRT/2 SIDE	I	When RW/SEEK is in RW, this becomes WPRT and indicates that the drive or media cannot be written data. When RW/SEEK is SEEK, becomes 2 SIDE and indicates that a double-sided media is inserted into the drive.
INDEX	I	Indicates a physical starting point on the track of the media.

Pin Name	I/O	Description
FLT/TRK0	I	When RW/SEEK is in RW, this becomes FLT and indicates that the drive is FAULT. When RW/SEEK is SEEK, becomes TRK0 and indicates that the R/W head of the drive is at cylinder 0.
TC	I	Indicates that read or write operation of the main system has been completed.
WDATA	O	Data to be written to the drive. Consists of clock bit and data bit.
WE	O	Makes the drive to write data.
WCLK	I	A timing signal for data to be written by the drive: 8MHz operation: FM — 500kHz, MFM — 1MHz 4MHz operation: FM — 250kHz, MFM — 500 kHz
PS0, 1	O	When writing in MFM mode, this determines whether the transfer speed of written data is to be advanced or delayed for obtaining a margin in load operation of the drive.
RDATA	I	Read data from the drive. Consists of clock bit and data bit.
WINDOW	I	Emitted from the VFO circuit and used to sample the RDATA. A phase synchronization between the data bit of the RDATA signal and WINDOW signal is made at the FDC.

Table 6-10

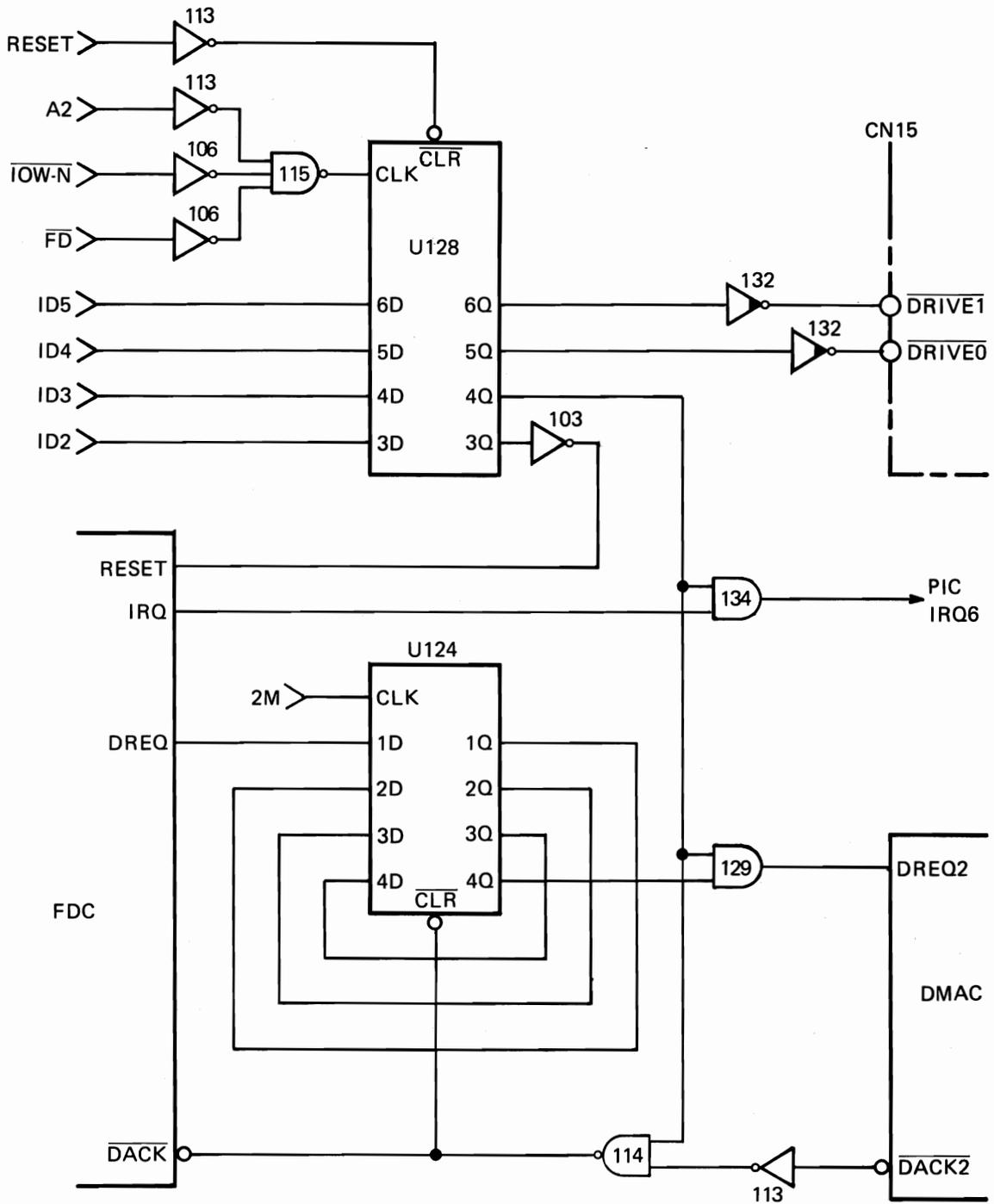


Figure 6-23

• Pre-Compensation Circuit

This circuit advances or delays write data for 125 nano seconds sent from the FDC to the FDD according to the data pattern. The FDC changes the status of the PS0 and PS1 terminals in response to a pattern of the write data sent from the CPU.

PS0	PS1	
L	L	Normal
L	H	Late
H	L	Early

When both PS0 and PS1 are LOW, an output from 2Q terminal of U126 is sent to the FDD as written data.

When PS0 is LOW and PS1 is HIGH, this status is called as Late mode. In this mode an output from 3Q terminal of U126 is sent to the FDD. This data is delayed for one clock cycle (125 nano seconds).

In Early mode - when PS0 is HIGH and PS1 is LOW - an output from 1Q terminal of U126 is sent to the FDD. This data is advanced for 1 clock cycle.

The SYNC signal of the FDC permits read operation at HIGH level, and inhibits at LOW.

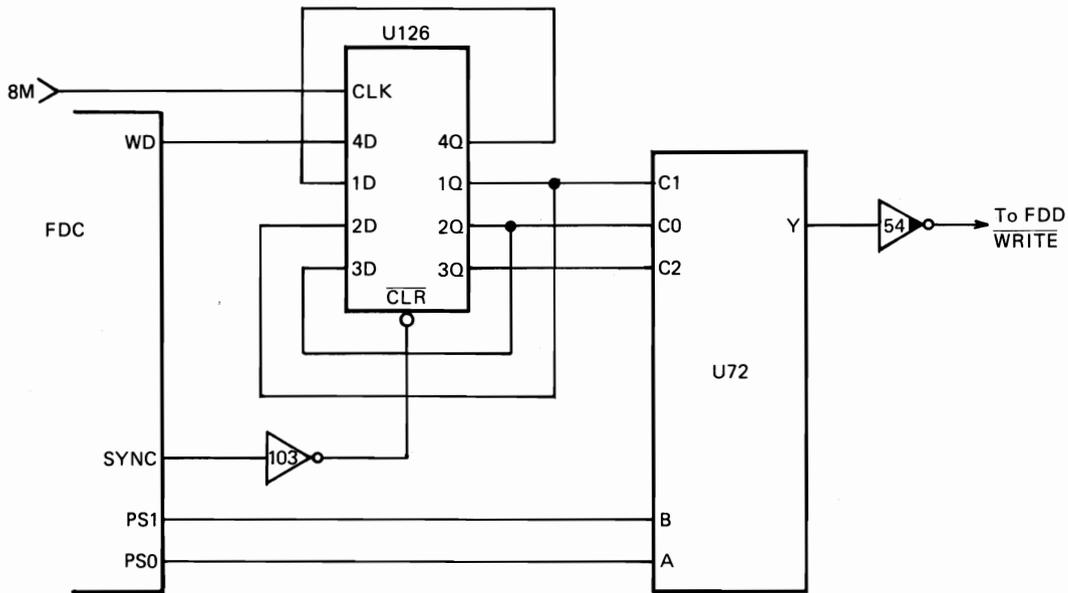


Figure 6-24

• **Data Separation Circuit**

The heart of this circuit is the VFO-IC, U104 (SED9420C0B).

The VFO emits the Window signal to separate data bits and clock bits from the data read from the FDD.

The FDC uses the data mode of the VFO at the MFM terminal.

When the output of the MFM terminal is LOW, it assigns FM mode and when HIGH, assigns MFM mode.

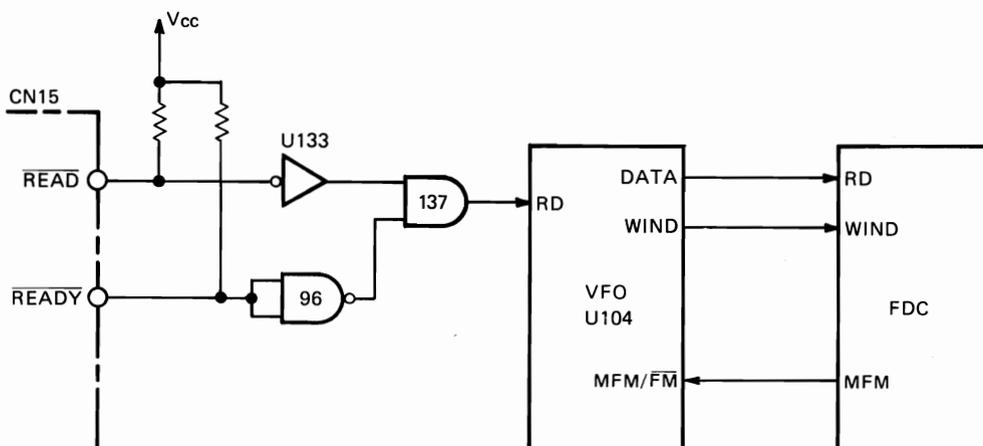


Figure 6-25

VI-3. Keyboard Unit

Figure 6-26 is a block diagram for the keyboard unit.

This unit employs 8048 (or 8784) 8-bit one chip microprocessor and is not synchronized with the main PCB.

The 8048 (or 8784) has 64-byte RAM and 1K-byte ROM. The RAM is used as the key buffer and the ROM contains the control programs including the self-diagnostics.

Signal P10 through P17 and P20 through P22 in the figure are used as key scan signals, and DB0 through DB7 is used as key return signals.

Interface between the main PCB is done at P23, P27, T0 and T1 terminals. P23 transmits a key clock signal, P27 also transmits a key data.

The CPU checks the T0 terminal to judge whether a key clock signal is output or not. This is to detect "soft reset" status that the keyboard interface on the main PCB shows by making the key clock signal line to LOW level for 20 milli seconds.

Similarly, the T1 terminal is used for the CPU to judge whether the buffer in the keyboard interface on the main PCB is full or not.

When the buffer in the keyboard interface is full, the keyboard interface will force the key data signal line to make LOW level.

The CPU sends the key scan signals to the key matrix and judges conditions for every key by reading the key return signals.

If any one of the keys is pressed, the CPU emits a key code signal corresponding to that key and sends it to the main PCB together with a key clock signal sequentially.

At this time, the CPU sends 7-bit key code and also 1-bit condition code which tell the condition of every keys.

When a key is changing from OFF to ON, the bit is LOW and changing from ON to OFF, HIGH. Table 6-11 is key code table.

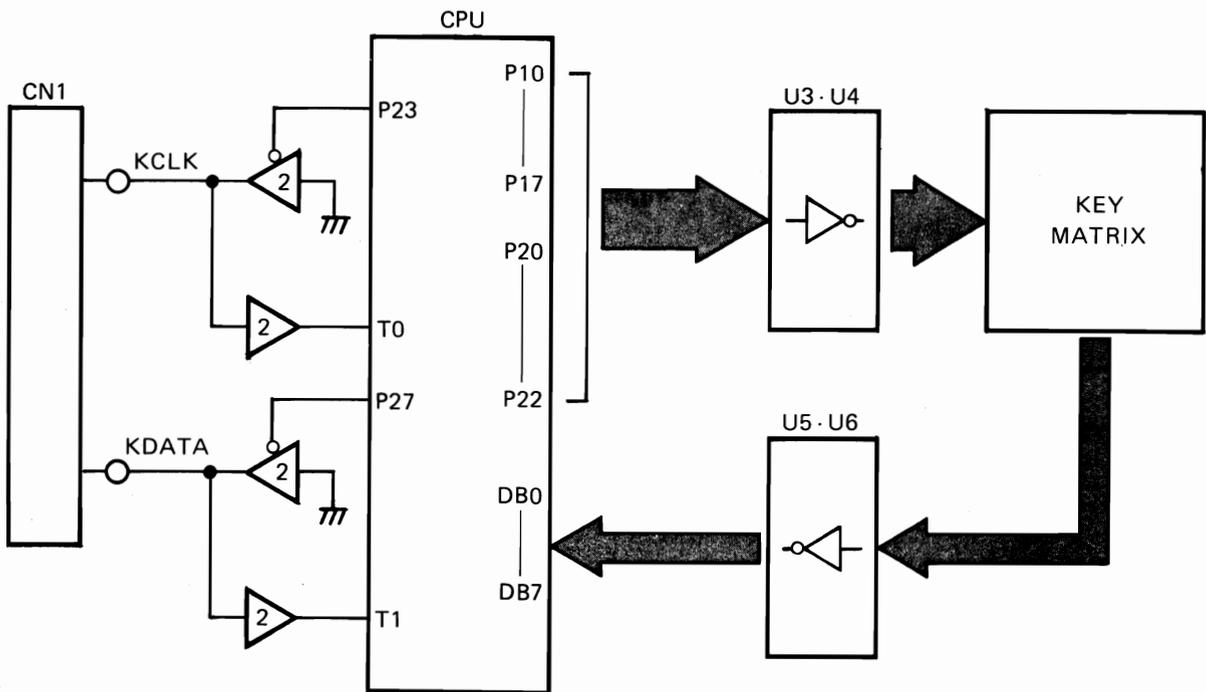


Figure 6-26

Figure 6-27 shows timing chart for key scanning.

One cycle of key scanning takes 800 micro seconds and following it, a 10 milli seconds of waiting time is employed. This is for avoiding a chattering. The CPU reperfoms one cycle of key scanning again and emits a key code signal in response to that two cycles of key scanning. If first and second data are identical, CPU assumes that the key have been pressed. In this way, the CPU avoids a chattering.

Figure 6-28 is the timing chart when the CPU transmits key data to the main PCB.

First, the CPU makes key data to HIGH level, reads these levels at T0 and T1 terminal and then checks whether the keyboard interface on the main PCB have been made this line to LOW level or not.

Next, the CPU sends 1 bit of HIGH level data (start bit) to the keyboard interface to initialize it. And finally, sends an 8-bit key code to the interface.

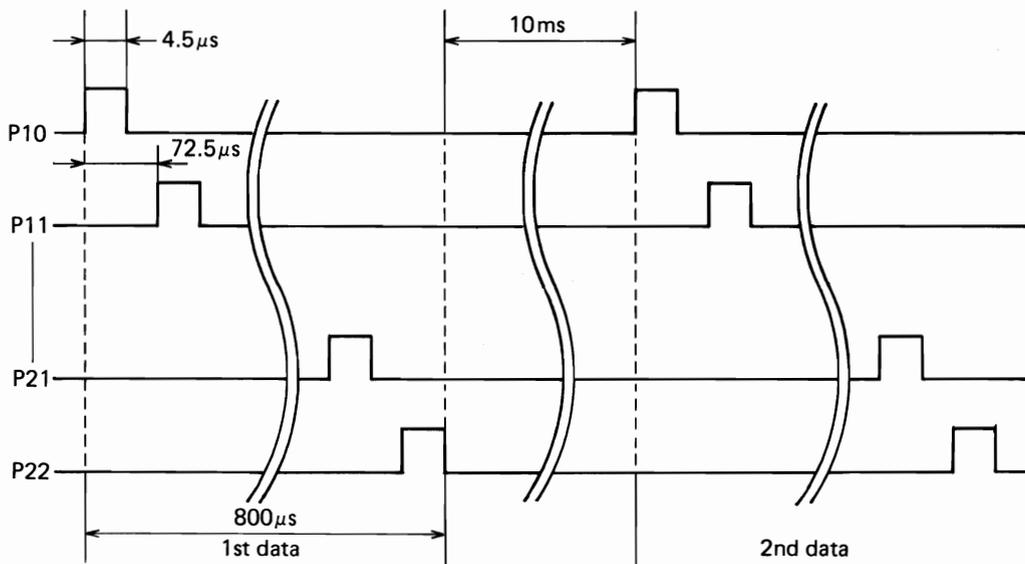


Figure 6-27

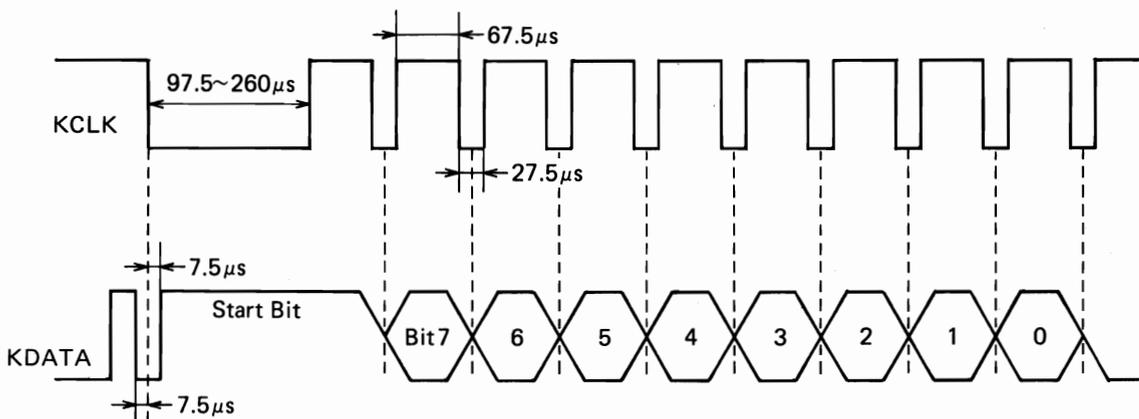


Figure 6-28

Key Code Table 1

ASCII

Key No.	Key Code	Key Name	Key No.	Key Code	Key Name
1	01	ESC	43	2B	\
2	02	1 !	44	2C	Z
3	03	2 @	45	2D	X
4	04	3 #	46	2E	C
5	05	4 \$	47	2F	V
6	06	5 %	48	30	B
7	07	6 ^	49	31	N
8	08	7 &	50	32	M
9	09	8 *	51	33	, <
10	0A	9 (52	34	. >
11	0B	0)	53	35	/ ?
12	0C	- _	54	36	SHIFT
13	0D	= +	55	37	PRTSCL *
14	0E	←	56	38	ALT
15	0F	← →	57	39	SPACE
16	10	Q	58	3A	CAPSLOCK
17	11	W	59	3B	F1
18	12	E	60	3C	F2
19	13	R	61	3D	F3
20	14	T	62	3E	F4
21	15	Y	63	3F	F5
22	16	U	64	40	F6
23	17	I	65	41	F7
24	18	O	66	42	F8
25	19	P	67	43	F9
26	1A	[{	68	44	F10
27	1B] }	69	45	NUM LOCK
28	1C	↵	70	46	SCROLL LOCK
29	1D	CTRL	71	47	7 HOME
30	1E	A	72	48	8 ↑
31	1F	S	73	49	9 PGUP
32	20	D	74	4A	-
33	21	F	75	4B	4 ←
34	22	G	76	4C	5
35	23	H	77	4D	6 →
36	24	J	78	4E	+
37	25	K	79	4F	1 END
38	26	L	80	50	2 ↓
39	27	; :	81	51	3 PGDN
40	28	, "	82	52	INS 0
41	29	· ~	83	53	DEL .
42	2A	SHIFT			

Table 6-11-a

Key Code Table 2

U.K.

Key No.	Key Code	Key Name	Key No.	Key Code	Key Name
1	01	ESC	43	2B	\
2	02	1 !	44	2C	Z
3	03	2 "	45	2D	X
4	04	3 £	46	2E	C
5	05	4 \$	47	2F	V
6	06	5 %	48	30	B
7	07	6 ^	49	31	N
8	08	7 &	50	32	M
9	09	8 *	51	33	, <
10	0A	9 (52	34	. >
11	0B	0)	53	35	/ ?
12	0C	- _	54	36	SHIFT
13	0D	= +	55	37	PRTSC *
14	0E	←	56	38	ALT
15	0F	← →	57	39	SPACE
16	10	Q	58	3A	CAPSLOCK
17	11	W	59	3B	F1
18	12	E	60	3C	F2
19	13	R	61	3D	F3
20	14	T	62	3E	F4
21	15	Y	63	3F	F5
22	16	U	64	40	F6
23	17	I	65	41	F7
24	18	O	66	42	F8
25	19	P	67	43	F9
26	1A	[{	68	44	F10
27	1B] }	69	45	NUM LOCK
28	1C	↵	70	46	SCROLL LOCK
29	1D	CTRL	71	47	7 HOME
30	1E	A	72	48	8 ↑
31	1F	S	73	49	9 PGUP
32	20	D	74	4A	-
33	21	F	75	4B	4 ←
34	22	G	76	4C	5
35	23	H	77	4D	6 →
36	24	J	78	4E	+
37	25	K	79	4F	1 END
38	26	L	80	50	2 ↓
39	27	; :	81	51	3 PGDN
40	28	' @	82	52	INS 0
41	29	# ~	83	53	DEL .
42	2A	SHIFT			

Table 6-11-b

Key Code Table 3

GERMAN

Key No.	Key Code	Key Name	Key No.	Key Code	Key Name
1	01	ESC	43	2B	< >
2	02	1 !	44	2C	Y
3	03	2 "	45	2D	X
4	04	3 §	46	2E	C
5	05	4 \$	47	2F	V
6	06	5 %	48	30	B
7	07	6 &	49	31	N
8	08	7 '	50	32	M
9	09	8 (51	33	, ;
10	0A	9)	52	34	. :
11	0B	0 =	53	35	- _
12	0C	B ?	54	36	SHIFT
13	0D	" '	55	37	PRTSC *
14	0E	←	56	38	ALT
15	0F	← →	57	39	SPACE
16	10	Q	58	3A	CAPSLock
17	11	W	59	3B	F1
18	12	E	60	3C	F2
19	13	R	61	3D	F3
20	14	T	62	3E	F4
21	15	Z	63	3F	F5
22	16	U	64	40	F6
23	17	I	65	41	F7
24	18	O	66	42	F8
25	19	P	67	43	F9
26	1A	Ü	68	44	F10
27	1B	+ *	69	45	NUM LOCK
28	1C	↵	70	46	SCROLL LOCK
29	1D	CTRL	71	47	7 HOME
30	1E	A	72	48	8 ↑
31	1F	S	73	49	9 PGUP
32	20	D	74	4A	-
33	21	F	75	4B	4 ←
34	22	G	76	4C	5
35	23	H	77	4D	6 →
36	24	J	78	4E	+
37	25	K	79	4F	1 END
38	26	L	80	50	2 ↓
39	27	Ö	81	51	3 PGDN
40	28	Ä	82	52	INS 0
41	29	# ~	83	53	DEL .
42	2A	SHIFT			

Table 6-11-c

Key Code Table 4

FRENCH

Key No.	Key Code	Key Name	Key No.	Key Code	Key Name
1	01	ESC	43	2B	< >
2	02	& 1	44	2C	W
3	03	é 2	45	2D	X
4	04	" 3	46	2E	C
5	05	' 4	47	2F	V
6	06	(5	48	30	B
7	07	§ 6	49	31	N
8	08	è 7	50	32	, ?
9	09	! 8	51	33	; .
10	0A	Ç 9	52	34	: /
11	0B	á 10	53	35	= +
12	0C) 11	54	36	SHIFT
13	0D	- 12	55	37	PRTSC *
14	0E	←	56	38	ALT
15	0F	← →	57	39	SPACE
16	10	A	58	3A	CAPSLOCK
17	11	Z	59	3B	F1
18	12	E	60	3C	F2
19	13	R	61	3D	F3
20	14	T	62	3E	F4
21	15	Y	63	3F	F5
22	16	U	64	40	F6
23	17	I	65	41	F7
24	18	O	66	42	F8
25	19	P	67	43	F9
26	1A	^ "	68	44	F10
27	1B	\$ *	69	45	NUM LOCK
28	1C	↵	70	46	SCROLL LOCK
29	1D	CTRL	71	47	7 HOME
30	1E	Q	72	48	8 ↑
31	1F	S	73	49	9 PGUP
32	20	D	74	4A	-
33	21	F	75	4B	4 ←
34	22	G	76	4C	5
35	23	H	77	4D	6 →
36	24	J	78	4E	+
37	25	K	79	4F	1 END
38	26	L	80	50	2 ↓
39	27	M	81	51	3 PGDN
40	28	ù %	82	52	INS 0
41	29	μ £	83	53	DEL
42	2A	SHIFT			

Table 6-11-d

VI-4. Display Adapter Boards

The A-200 is equipped with monochrome or color display adaptor board as the standard. Namely, Model M1 and M2 have the monochrome board, and Model C1 and C2 have the color board. Either adaptor boards are controlled by the 68B45 CRTIC.

VI-4-1. Pin Description of the 68B45

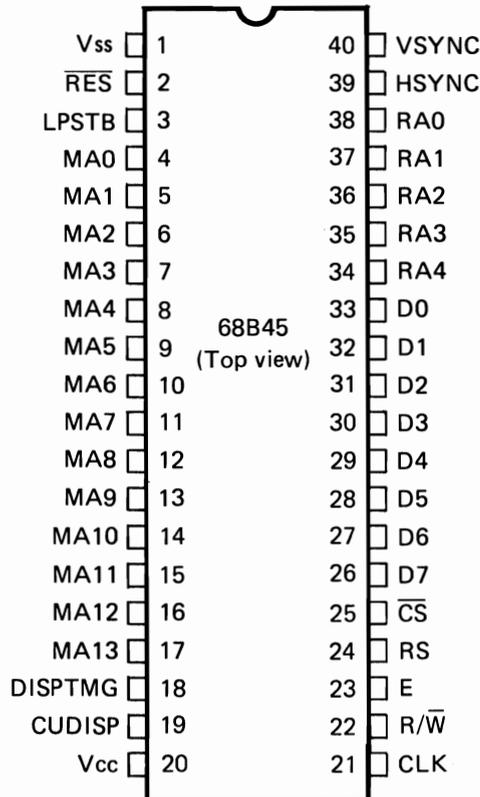


Figure 6-29

- D0 — D7: bi-directional data bus

These terminals are used when transferring data between the CRTIC and the CPU. These outputs turn three state buffer.

Unless the CPU reads the contents of the register of the CRTIC, this bus remains high-impedance.

- R/W (Read/Write)

This signal controls a direction of data transferring between the CRTIC and the CPU. That is, when this signal is HIGH, a data from the CRTIC is transferred to the CPU, and when LOW, a data from the CPU is transferred to the CRTIC.

- CS (Chip Select)

Only when the CS signal is LOW, the CPU can access internal registers of the CRTIC.

- RS (Register Set)

This signal is used when dividing the internal one address register and 18-control registers. That is, when this terminal is LOW the address register is selected, and when HIGH the control registers is selected.

- E (Enable)

This signal is used as a strobe signal when the CPU reads from or writes to the internal registers of the CRTIC.

- **$\overline{\text{RES}}$ (Reset)**

This signal resets the CRTC externally. When this terminal is LOW, following things will occur:

1. The counter in the CRTC will be reset and stops operation.
2. All output signals other than D0 through D7 signals become LOW.
3. The status of both address and control registers do not affect with the $\overline{\text{RES}}$ signal. The CPU can access these registers even when the CRTC is in RESET mode.

- **CLK (Character Clock)**

This terminal is the fundamental clock input for any operation of the CRTC.

- **HSYNC (Horizontal Synchronous)**

This terminal outputs the H-sync. signal to the CRT.

- **VSYNC (Vertical Synchronous)**

This terminal outputs the V-sync. signal to the CRT.

- **DISPTMG (Display Timing)**

This signal denotes one screen displaying period of the H-sync. and V-sync signals.

- **MA0 — MA13: Refresh Memory Address**

These signals are memory address outputs for refreshing an information on the CRT at certain period of time.

As for the color display adaptor board, the CRTC supports 8-display pages.

- **RA0 — RA4: Raster Address**

This signal is a raster select signal for the character generator.

- **CUDISP (Cursor Display)**

This video signal is used for displaying a cursor sign on the CRT monitor. It is inhibited when the DISPTMG signal is LOW.

VI-4-2. Monochrome Display Adaptor Board

The monochrome display adaptor board is equipped with the A-200 Model M1 and M2. Generally, this board has following specifications.

- * Displays 80 × 25 characters in one screen
- * 9 × 14 pixels for one character box
- * 7 × 9 pixels for one character
- * Can drive an 18kHz-monochrome display monitor
- * With character attribute
- * Can display 256 different characters
- * Video signal: 16.257MHz maximum
- * V-sync signal: 720 x 350 (H x V), 50Hz
- * H-sync signal: 18.432kHz

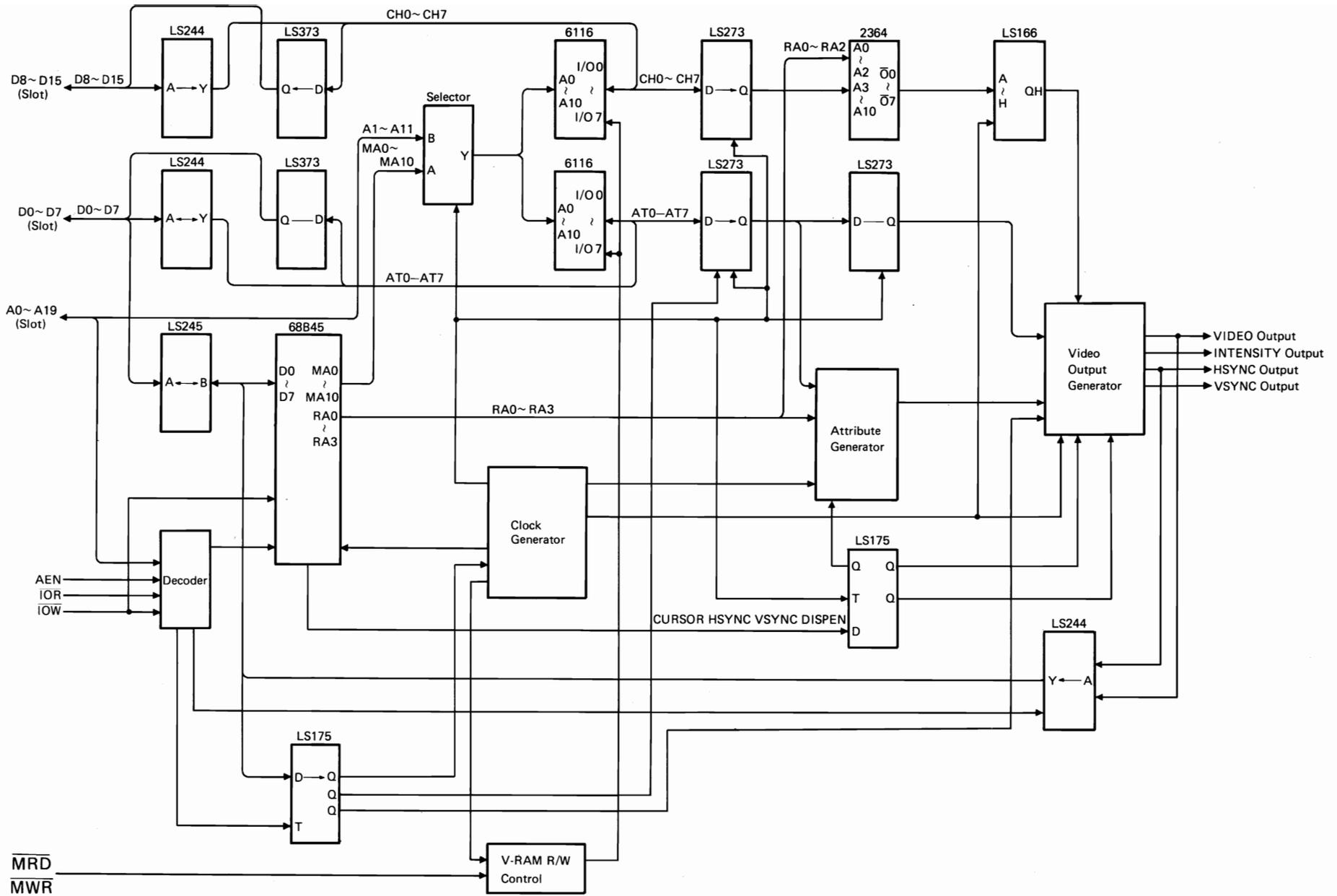
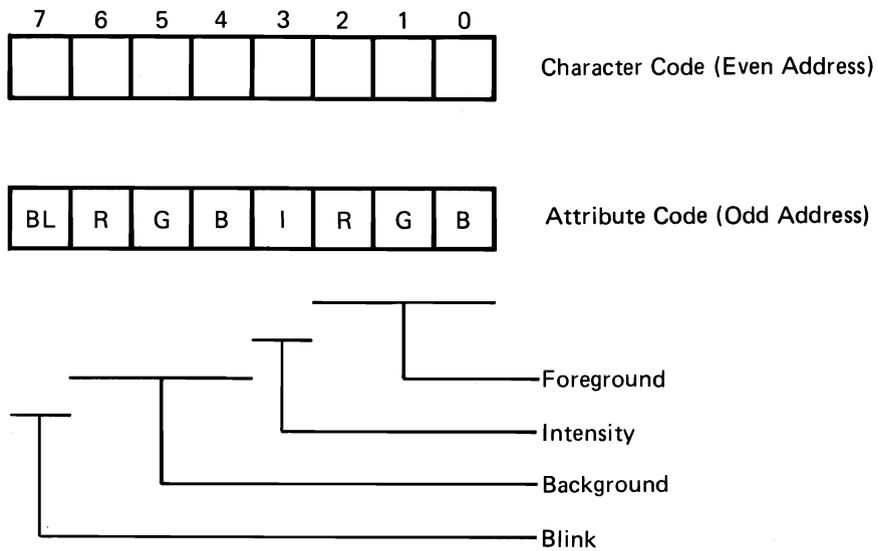


Figure 6-30

• **Character**

Every character to be displayed has one byte of character code and also one byte of attribute code. An attribute byte can be divided into four functions: blink, intensity, foreground and background. Their assignments are illustrated as follows.



Background			Foreground			Display mode
R	G	B	R	G	B	
0	0	0	0	0	0	Non display
0	0	0	0	0	1	With underline
0	0	0	1	1	1	Normal display
1	1	1	0	0	0	Reverse display

Table 6-12

Blink	Display mode	Intensity	Display mode
0	Non blink	0	Normal intensity
1	Blink	1	High intensity

Table 6-13

- **V-RAM**

The monochrome display adapter board has 4K bytes of V-RAM.

2K of 4K bytes store character codes corresponding to the characters to be displayed on the screen, and other 2K bytes are used for storage of attribute codes. Unlike the system RAM on the main board, the V-RAM has no parity bits.

The V-RAM area is assigned at the address B0000H and upper.

I/O Address	Description
3B4	68B45 Index register
3B5	68B45 Data register
3B8	CRT Control port
3BA	CRT Status port

Table 6-14

Further, 3B8 and 3BA are assigned as follows:

I/O Address	Bit	Description
3 B 8	0	High resolution mode
	3	Video enable
	6	Blink enable

Table 6-15

Unless the address 3B8 is "01", OSC signal is not output and as a result, nothing is displayed on the screen.

I/O Address	Bit	Description
3BA	0	H-sync
	3	B/W video

Table 6-16

This port is used to check the monochrome display adaptor board. That is, whether the H-sync or B/W video signal is output or not is judged through this port.

• Clock Generator Circuit

This circuit that is illustrated in the figure below generates a fundamental clock signal for controlling the display adapter itself and a display monitor.

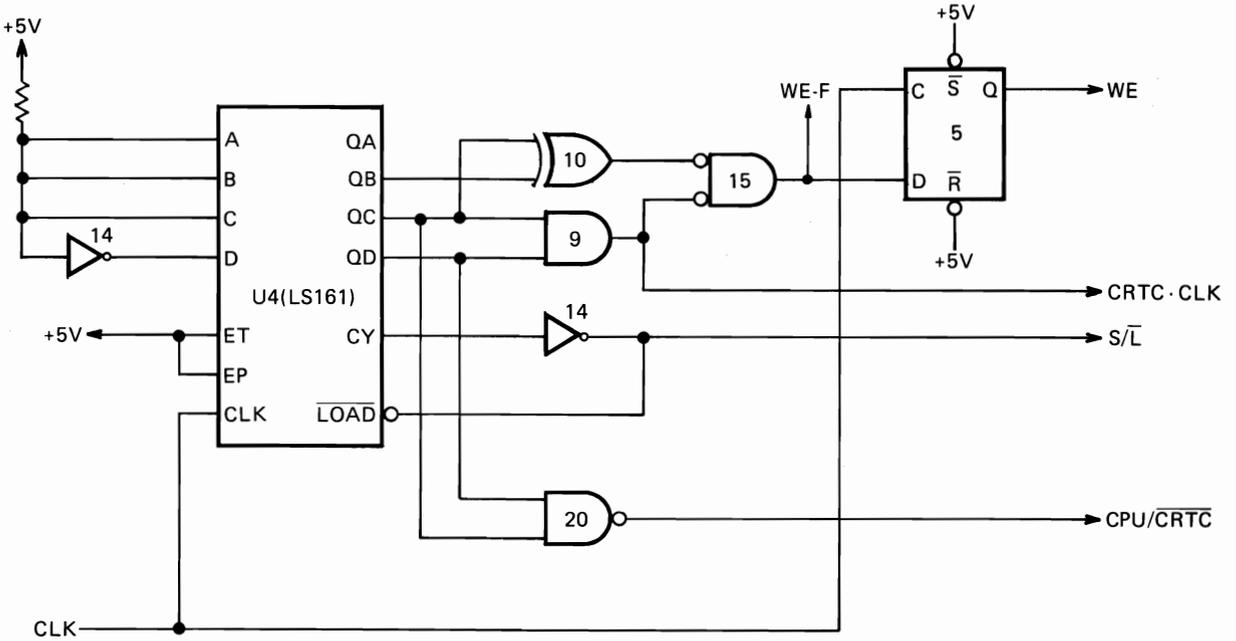


Figure 6-31

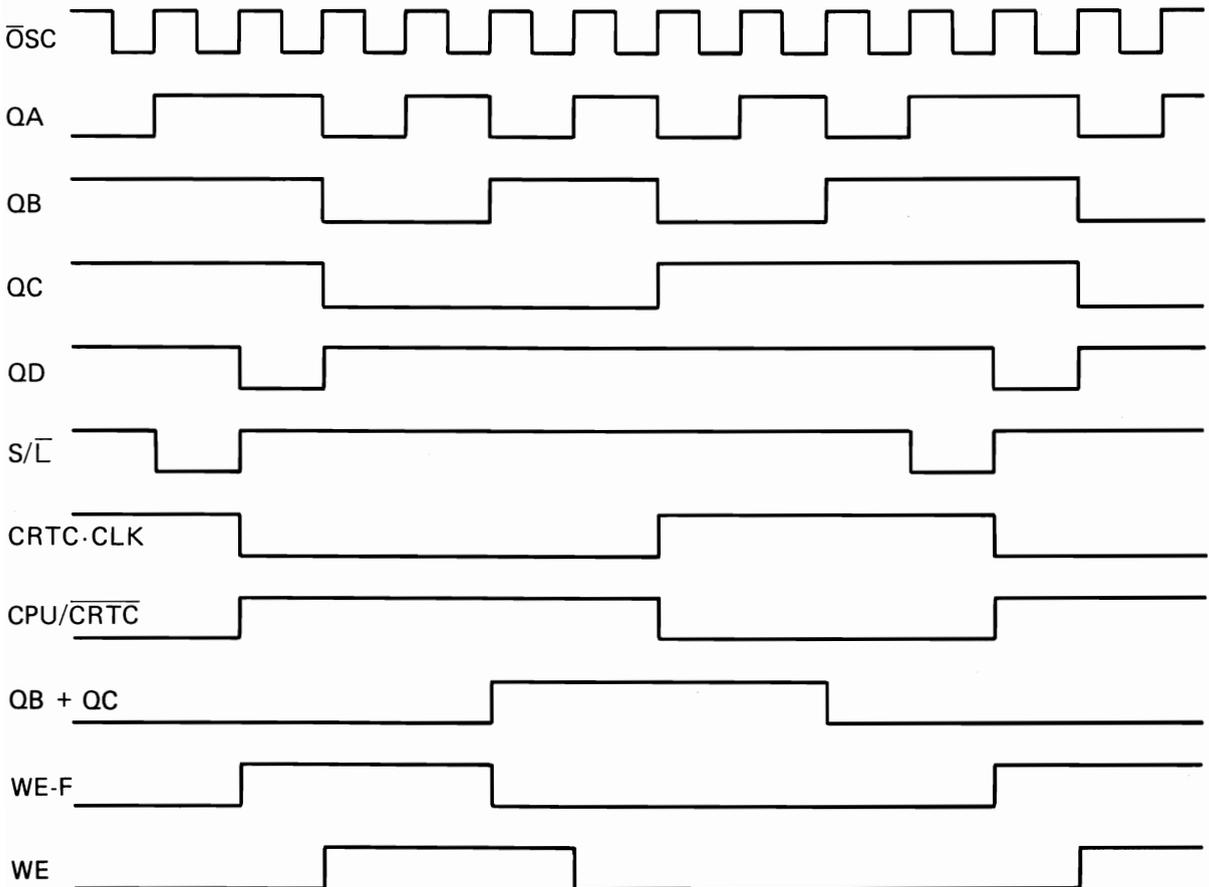


Figure 6-32

The heart of this circuit is the LS161 Synchronous Counter.

When the all output terminals QA, QB, QC and QD become HIGH, a HIGH level signal is output from the CY terminal and then a inverted LOW level signal is input to the \overline{LOAD} terminal. In this case, values at the A, B, C and D terminals are input and then they are output at a rising edge of the next clock cycle. Further, these values are counted up at the every following clock cycle. The fundamental clock signals for this display board is made using these output signals. Detailed description for every clock signal is as follows:

CRTC-CLK

This signal is emitted by ANDing the QC and QA output signals and is fed to the CRTC.

CPU/ \overline{CRTC}

This clock is made by NANDing the QC and QD outputs and switches the addresses of the V-RAM between the CPU mode and CRTC mode. In the CRTC mode, this signal is used as the \overline{OE} signal, the attribute signal and the timing signal for latching of the character signals, etc.

S/ \overline{L}

The S/ \overline{L} signal is generated by inverting the CY signal and used as the load signal for the LS161 and for the character shift register (LS166).

WE

WE signal is generated by shifting a signal input to the D terminal of U5 for one clock cycle. The signal to be sent to the D terminal is made by NANDing the EX-ORed output of QB and QA and the CRTC-CLK signal. This WE signal becomes the writing signal to the V-RAM when the CPU cycle.

- **Attribute Generator**

Figure 6-33 is an overview of this circuit.

Descriptions for each output signal is as follows:

NON-DISP

This signal is made by decoding the attribute signals. That is, when the AT0, AT1, AT2, AT4, AT5 and AT6 signals are all LOW, the NON-DISP signal also becomes LOW. In this case, no character is displayed on the screen.

REVERSE

This signal is also made by decoding the attribute signals. When the AT0, AT1 and AT2 are LOW and the AT4, AT5 and AT6 is HIGH, the REVERSE signal becomes HIGH. In this case, the video signal becomes to the reverse mode.

UNDERLINE

When the attribute signals AT0 is HIGH, AT1, AT2, AT4, AT5 and AT6 are LOW, this signal is output. In this case, an underline sign previously set in the CRTC is output on the screen.

BLINK

When the AT7" signal is HIGH, the BLINK-EN signal is HIGH and the CURSOR signal is not active, the BLINK signal make the CRTC to generate a signal which is made by dividing the V-SYNC signal into one 32th. When this signal is LOW, displayed characters are disappear and when HIGH, re-appear.

CURSOR*

This signal is made by ANDing the CURSOR signal from the CRTC and a signal which is divided the V-SYNC signal into one 16th. This CURSOR signal is controlled by the software.

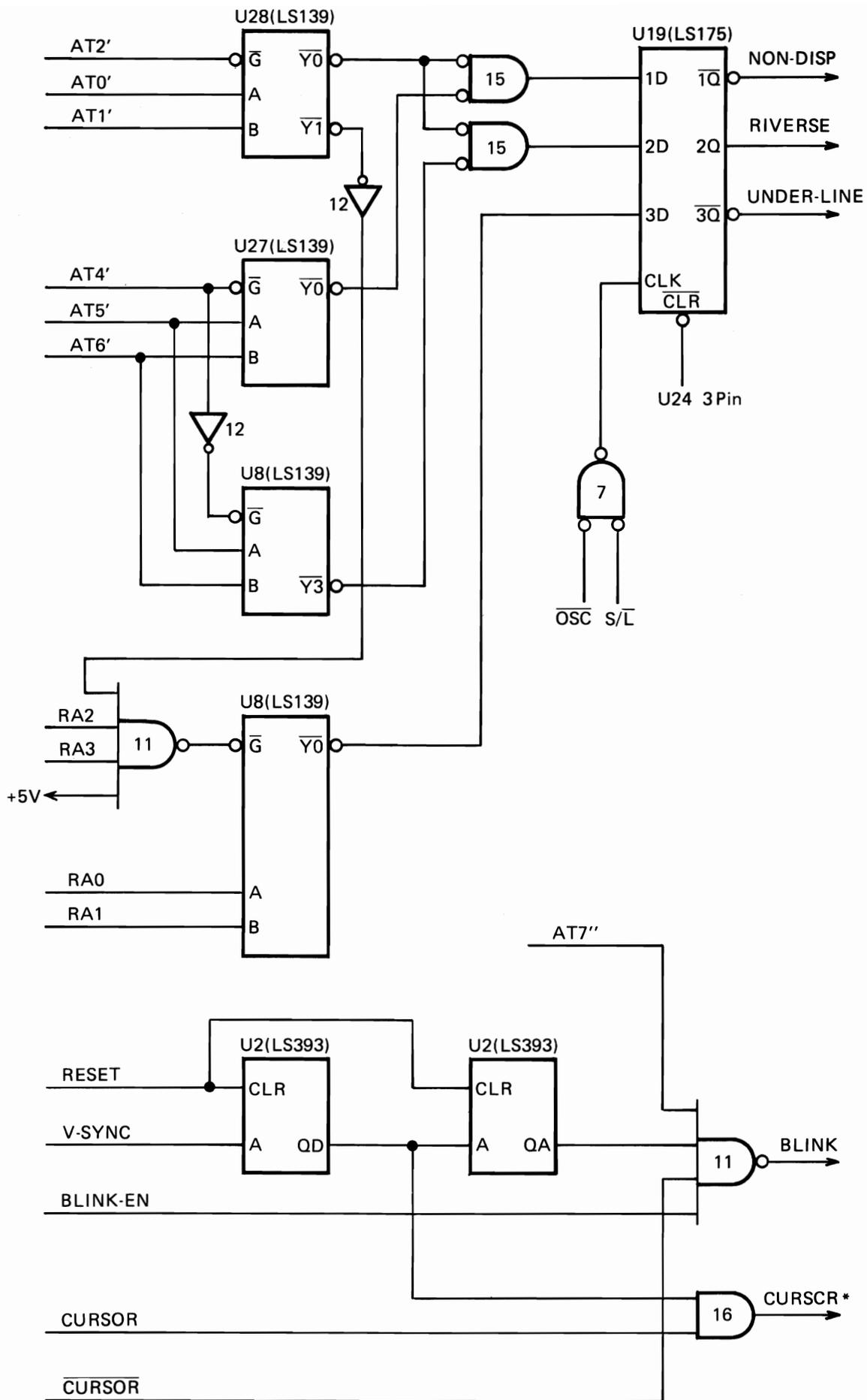


Figure 6-33

• Video Output Generator Circuit

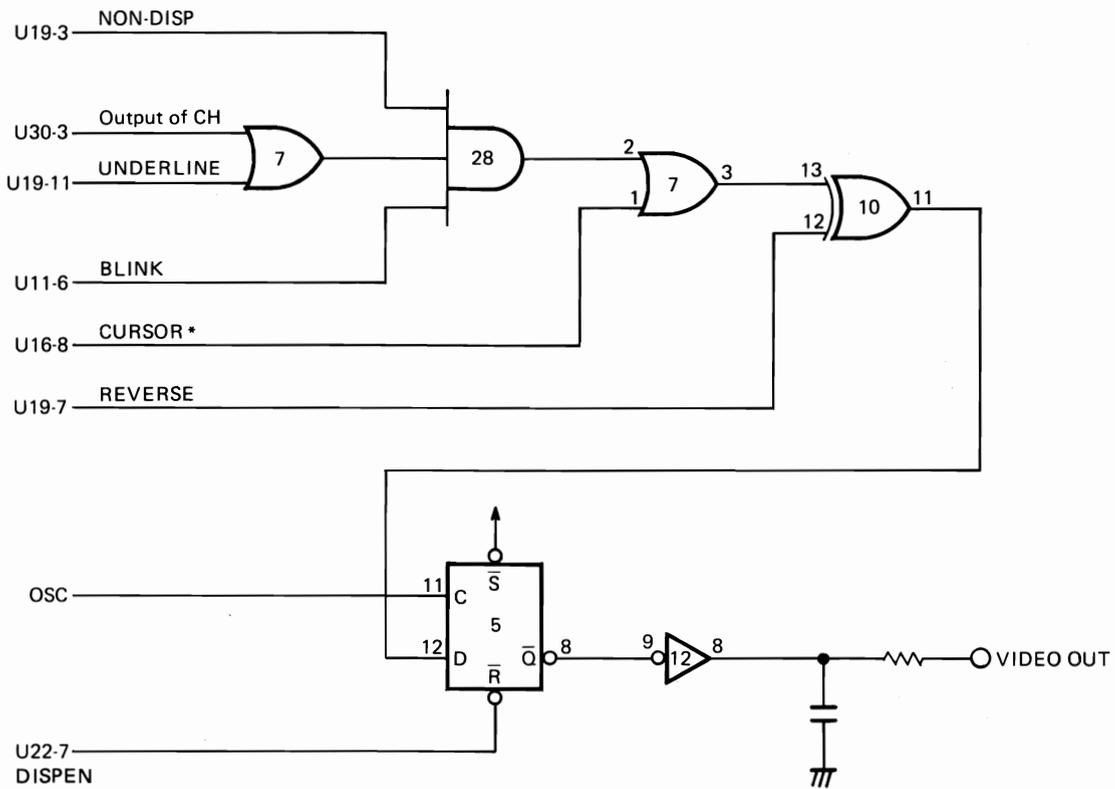


Figure 6-34

The figure above illustrates an overview of this circuit.

The character outputs shifted by the shift register (LS166) corresponding to every one pixel on the screen, is synchronized with the OSC clock signal after mixing with the attribute signal. As above illustration shows, the character output signal is ORed with the UNDERLINE signal. Namely, when either the character signal or the UNDERLINE signal is HIGH, the pin 6 of U7 becomes HIGH.

Next, the output of 6-pin is ANDed with the NON-DISP signal and the BLINK signal by U28. In this case, either one of these two signals is LOW, the output terminal of U28 (12-pin) becomes LOW.

Then this output signal is ORed with the CURSOR* signal by U7.

Finally, the output signal from the 3-pin of U7 is compared with the REVERSE signal by U10. Therefore, when the REVERSE signal is HIGH, the signal from the 3-pin of U7 is inverted at U10. Conversely, when the REVERSE signal is LOW, that output signal from U7 will be output from U10 as its logical level is unchanged.

- **V-RAM Read Timing**

1. When the CPU emits the $\overline{\text{MRD}}$ signal, the I/O READY signal becomes disabled and the CPU then becomes the wait state.
2. The pin 8 of U1 becomes HIGH at the falling edge of the $\text{S}/\overline{\text{L}}$ signal, and is reset at the rising edge of the next CRTC-CLK signal. When the signal from the pin 8 of U1 is HIGH and when this signal is accessing the V-RAM in the CPU cycle, the $\overline{\text{OE}}$ signal of the 6116 then becomes LOW.
3. Next, a data is output from the 6116. This data is latched at the rising edge of the I/O READY signal and simultaneously, it makes the I/O READY signal enable.
4. The CPU then reads the data which has been latched at the falling edge of the T4 cycle.
5. When the CPU enters into T4 cycle, the $\overline{\text{MRD}}$ signal becomes HIGH and an impedance of I/O READY signal keeps high.

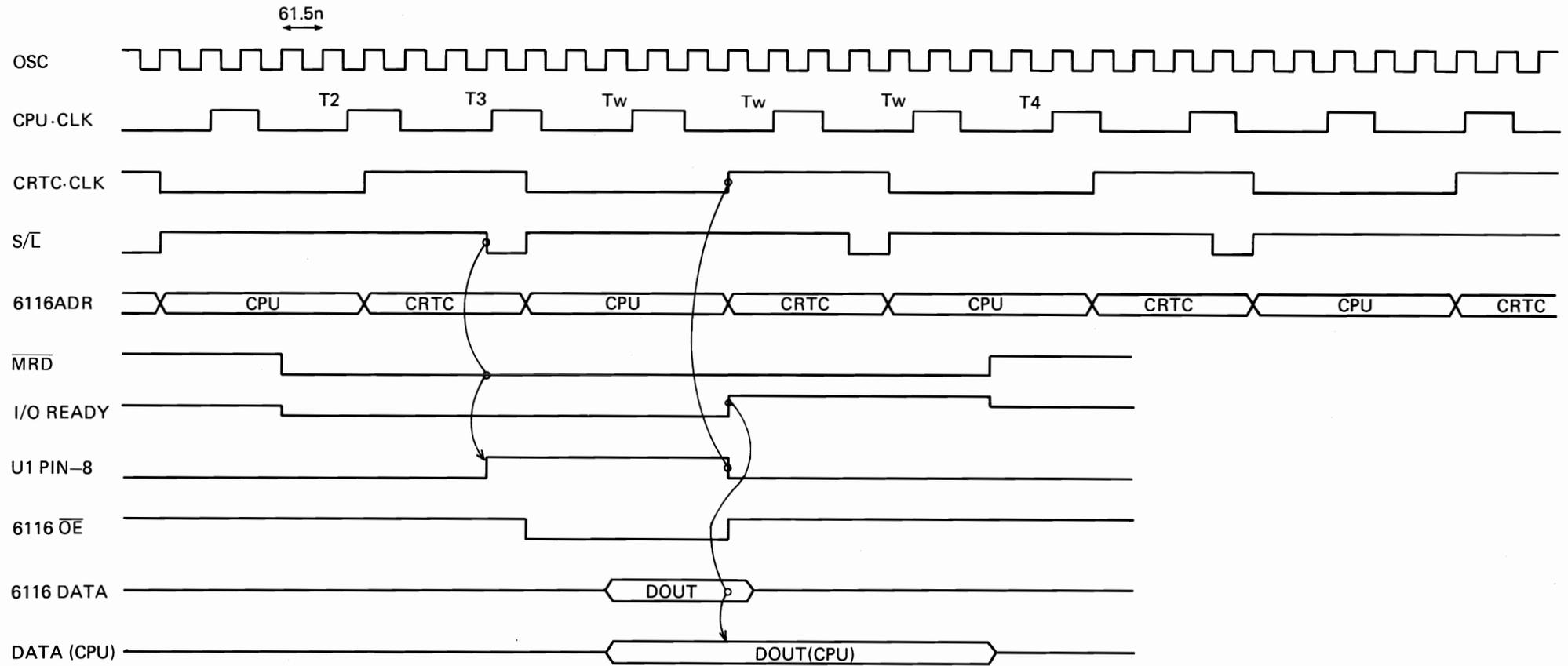


Figure 6-35

- **V-RAM Write Timing**

1. When the CPU emits the \overline{MWR} signal, the I/O READY signal becomes disabled, and the CPU then enters wait state.
2. The pin 8 of U1 becomes HIGH at the falling edge of the $\overline{S/L}$ signal. In this case, if the pin 5 of U5 is HIGH and the CPU is in memory write mode, the \overline{OE} signal of the 6116 becomes LOW.
Then the data sent from the CPU is written to the 6116.
3. The I/O READY signal becomes HIGH at the rising edge of the CRTIC-CLK signal. When the CPU cycle is changed from TW cycle to T4 cycle, the \overline{MWR} signal becomes HIGH. Then an impedance of the I/O READY signal becomes high.

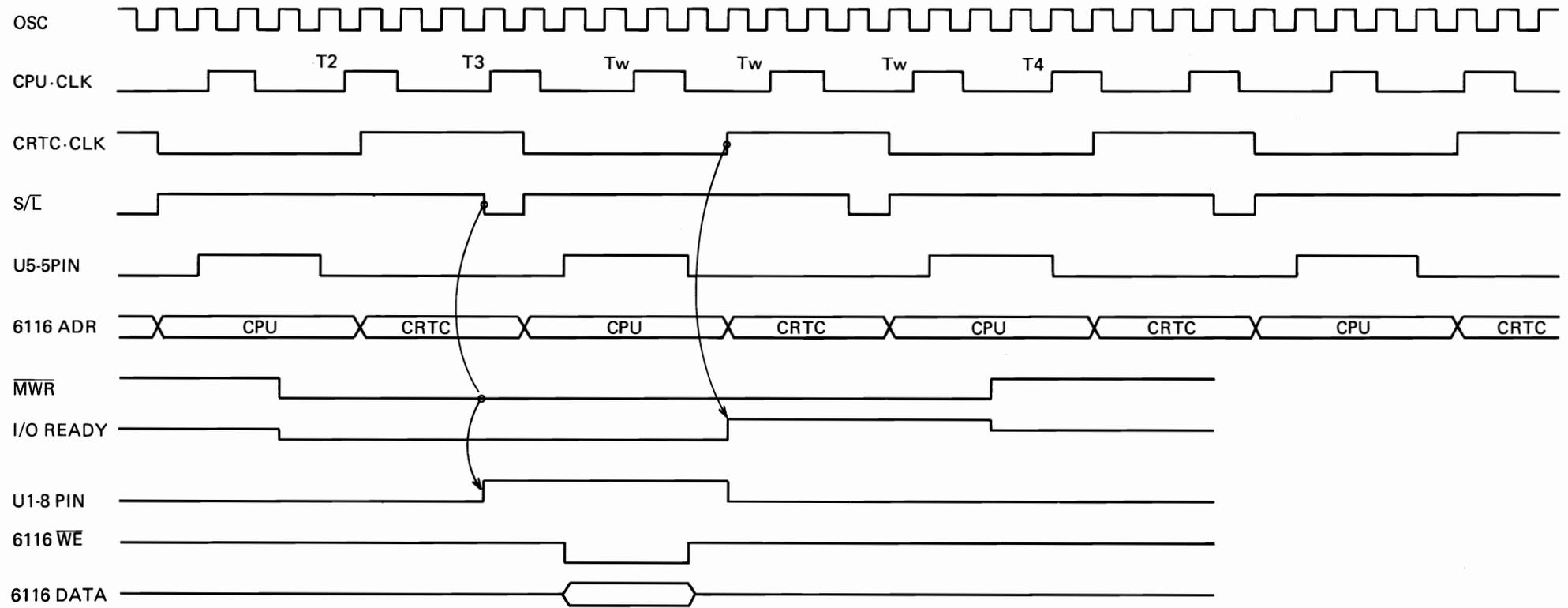


Figure 6-36

- **Video Output Timing**

The V-RAM is accessed by the CPU and the CRTC alternately. Switching between the CRT mode and the CRTC mode is performed by the CPU/CRTC clock signal.

When in the CRTC mode, the CPU/CRTC clock signal becomes the \overline{OE} signal to the 6116 and as a result, a data is output to the bus.

This data is latched at the rising edge of the CPU/CRTC clock signal and finally, this latched signal becomes an address for the Character Generator (2364).

Since the 2364 can always be accessed, it output a data on to the data bus when the address is determined. This data is input to the shift register (LS166) when the S/L signal is LOW, and is output at the next OSC clock after it is shifted corresponding to every one pixel on the screen.

As well as the CH (Character) signal, the AT (Attribute) signal is output when in the CRTC mode.

A data output from the 6116 is latched at rising edge of the CPU/CRTC clock signal.

A dot signal output from the shift register and this attribute signal are mixed and latched at the rising edge of the next OSC clock signal. This latched signal becomes the video output.

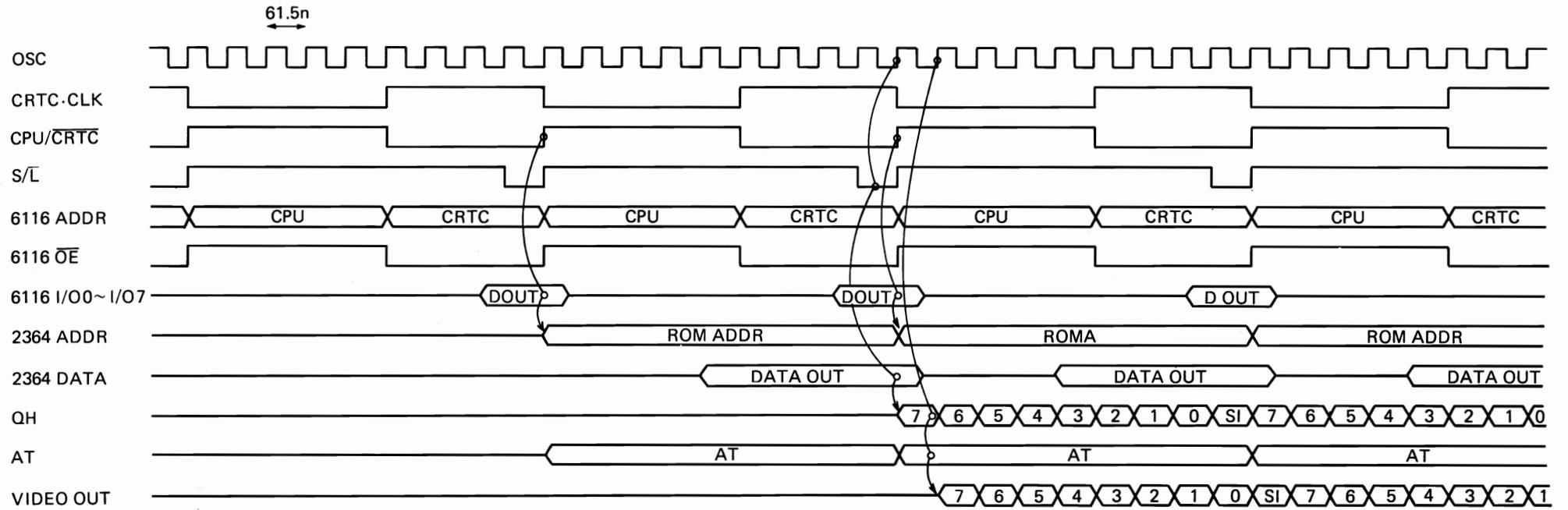


Figure 6-37

VI-4-3. Color Display Adaptor Board

The color display adaptor board is equipped with the A-200 Model C1 and C2. Not only it can display characters, but also supports a graphic screen.

This board has following specifications.

- * Displays 80 × 25 or 40 × 25 characters in one screen
- * 8 × 8 pixels for one character box
- * 7 × 7 pixels for one character
- * With character attribute
- * Can display 256 different characters
- * Video signal: 14.31818MHz maximum
- * V-sync signal: 60Hz
- * H-sync signal: 15.75kHz

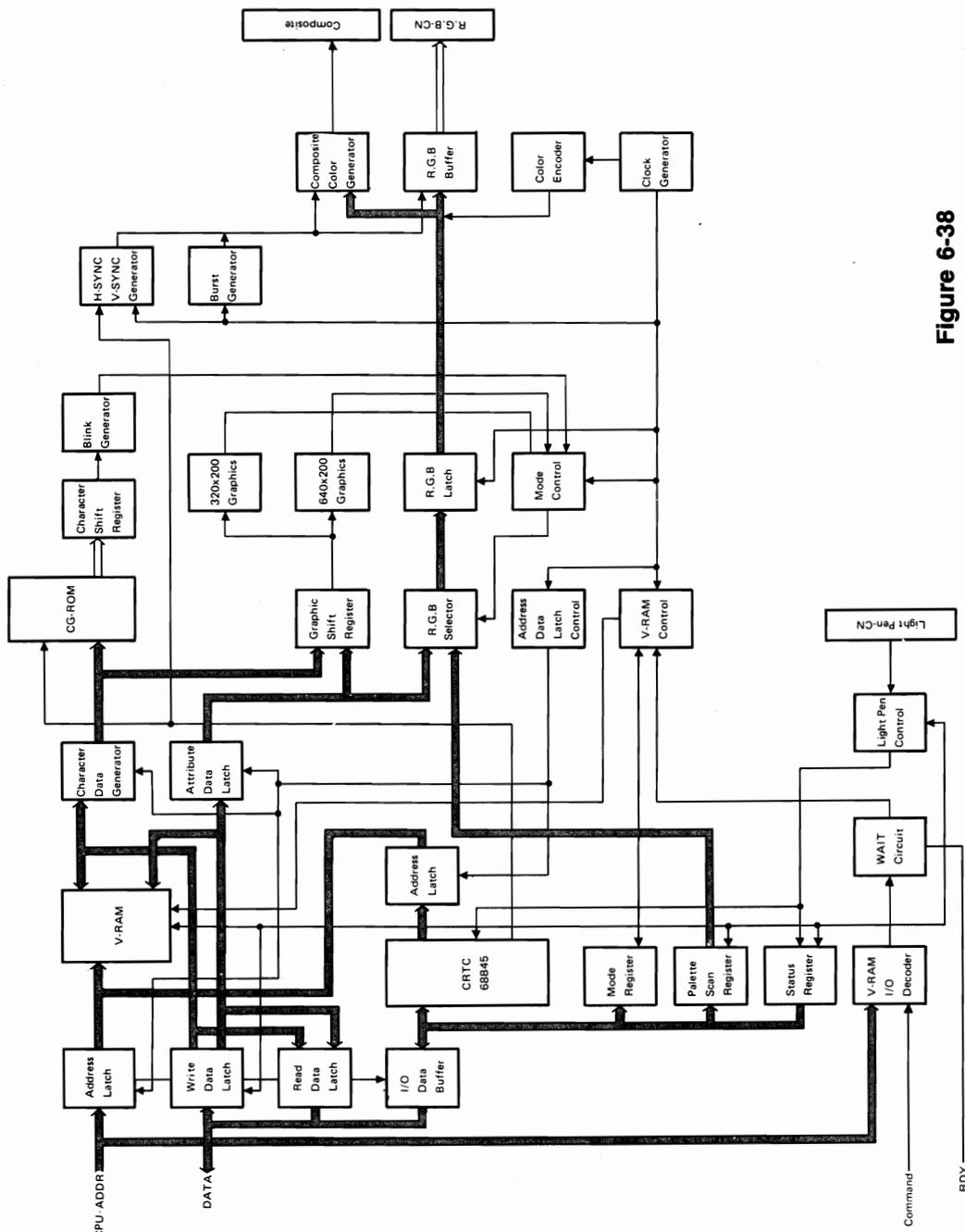
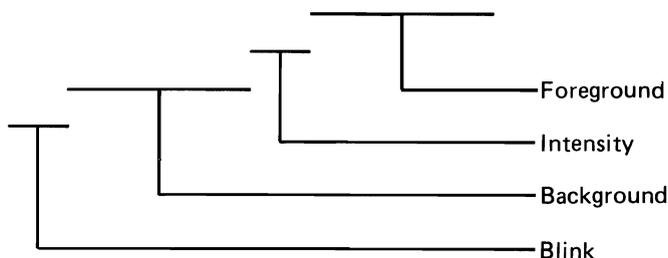
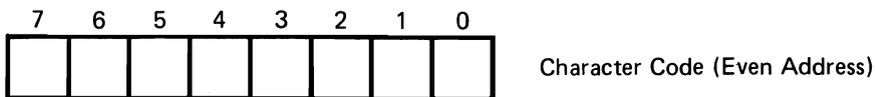


Figure 6-38

• **Character Mode**

Like the monochrome board, every character to be displayed has one byte of character code and also one byte of attribute code.

Functions of attribute byte are identical as the monochrome board.



• **320 × 200 Pixels Graphic Mode**

In this mode, 4 of 16 colors can be displayed.

Functional assignment for every byte are illustrated as follows.

7	6	5	4	3	2	1	0
C1	C0	C1	C0	C1	C0	C1	C0
First display element		Second display element		Third display element		Fourth display element	

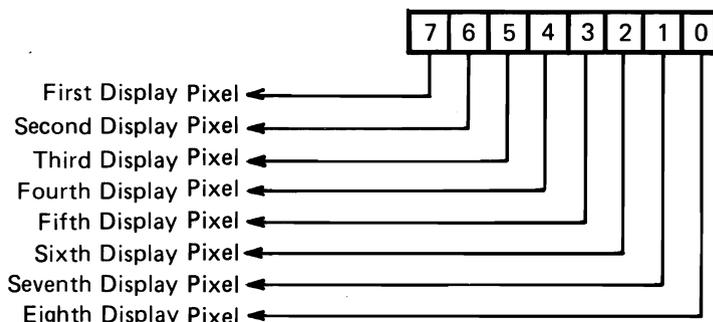
Table 6-17

Colors to be displayed are selected with C0 and C1 above.

The color selection is done by the IC U19 (LS174).

• **640 × 200 Pixels Graphics Mode**

In this high resolution mode, every bit of the V-RAM corresponds every pixel on the screen, and so, only a black and white mode display can be performed.



CPU/CRTC

This clock is selected by the HRES signal. Namely, when the screen is in 40 × 25 pixels text mode, an output signal of U65-2 pin is used as the CPU/CRTC signal, and when 80 × 25 pixels mode, an output of U39-6 pin is used.

CRT-CLK

This clock signal is also selected by the HRES signal. When the screen is in 40 × 25 pixels text mode, an output signal of U66-2 pin is used as the CRT-CLK signal and when 80 × 25 pixels mode, an inverted signal of U65-7 pin output is used.

The CRT-CLK controls the fundamental operations of the CRTC.

DOT-CLK

This signal is also selected by the HRES signal. When the screen is in 40 × 25 pixels text mode, an output signal of U65-10 pin is used as the DOT-CLK signal, and when 80 × 25 pixels mode, an inverted signal of the OSC signal (14.31818MHz).

This DOT-CLK signal is used as the timing clock for shifting the dot data in the character mode, or when the graphics mode, this signal is used as the latch clock of every bit.

S/L

This signal is selected by the HRES signal. When the screen is in 320 × 200 pixels of graphics mode, an Ex-ORed signal of U66-2 pin output and U65-5 pin output, and an NORed signal of U18-2 pin output and U66-5 pin output are ORed at U58, and this signal is used as the S/L signal. For 640 × 200 pixels screen, the cycle of the S/L signal is extended to a double, and used as the LOAD signal of the shift register which shifts the dot data in the graphics mode.

CAS

This signal is an ANDed signal of U64-2 pin output and U60-6 pin output. This clock is used for the V-RAM.

RAS

This signal is an Ex-ORed signal of U66-2 pin and U65-2 pin.

Further, the RAS signal is ANDed with the V-RAM decode signal and used as the RAS signal of the V-RAM.

*** Clock Timing**

80 × 25 or 40 × 25 Characters Text Mode

The address signal from the CRTC is output at the falling edge of the CRT-CLK clock signal. This address is latched at the rising edge of the RAS signal and then is divided into the row address and column address by the CRTC-RAS ADDR and CRTC-CAS ADDR signals. The row address is read at the falling edge of the RAS signal and the column address is read at the falling edge of the CAS signal. At the same time, data is output from the D-RAM. This data is latched at the falling edge of the CH-LATCH and the AT-LATCH signals.

Output signals of the U27 are used as the address signals of the character generator (2364) and outputs from the U28 are used as the attribute signals.

• Attribute Generator Circuit

The character data output from the CH shift register (U25; LS166) is ANDed with the U49-3 pin output at U41. This U49-3 pin signal is an ORed signal of U37-8 output which is an enable signal of blinking an U48-11 output which is divided the V-SYNC signal into a half. Therefore, when the output from U49-3 pin is HIGH, an information output from the QH terminal (pin 13 or U25) is also output from U49-11 pin as it is.

The signal from U49-11 pin is an ORed signal of U41-8 pin output and U56-10 pin output. This signal is selected by the U57 and then sent to the U49-9 pin. Further, the signal from U57-4 pin is input to both U33-14 pin and U34-14 pin. These two ICs add an information concerning an attribute to the character data and then output to U32 which synchronizes these outputs with the DOT-CLK signal.

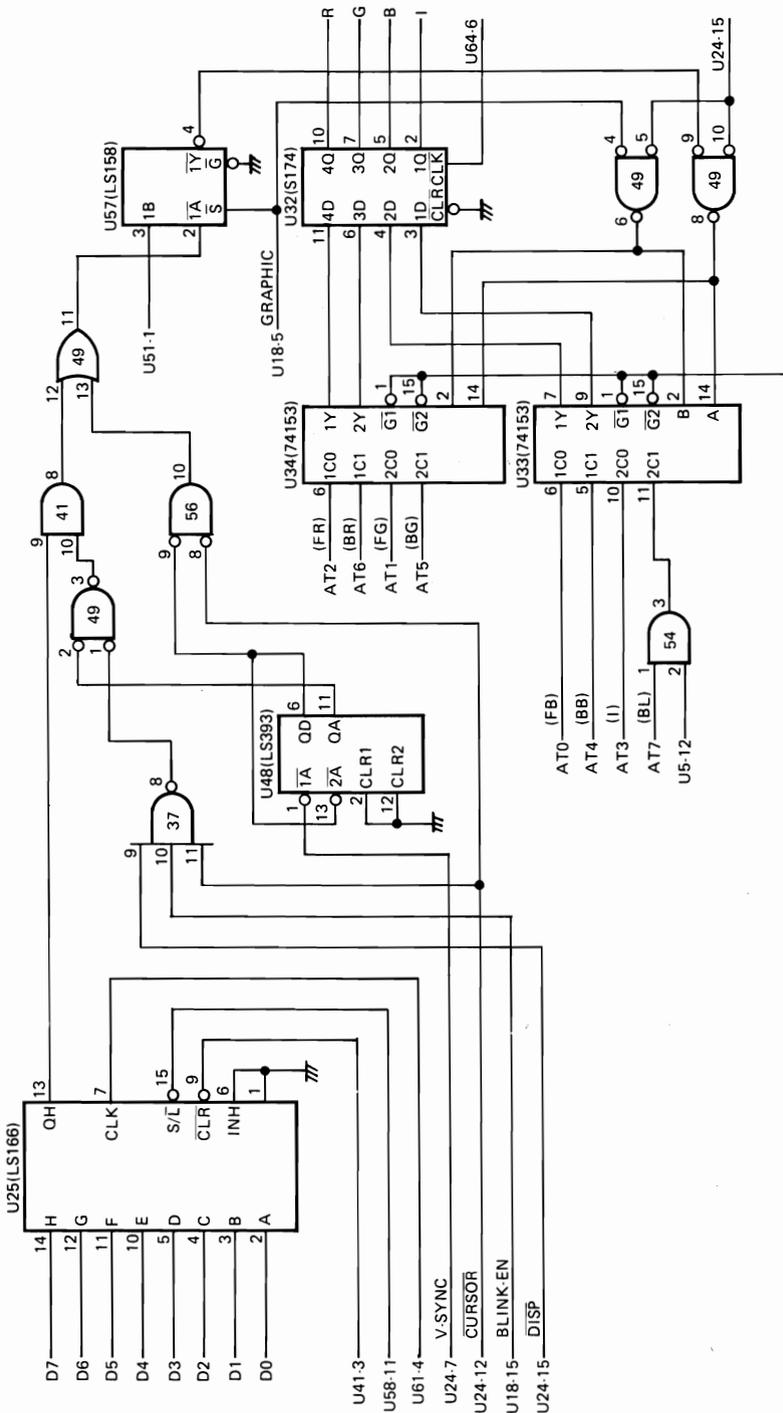
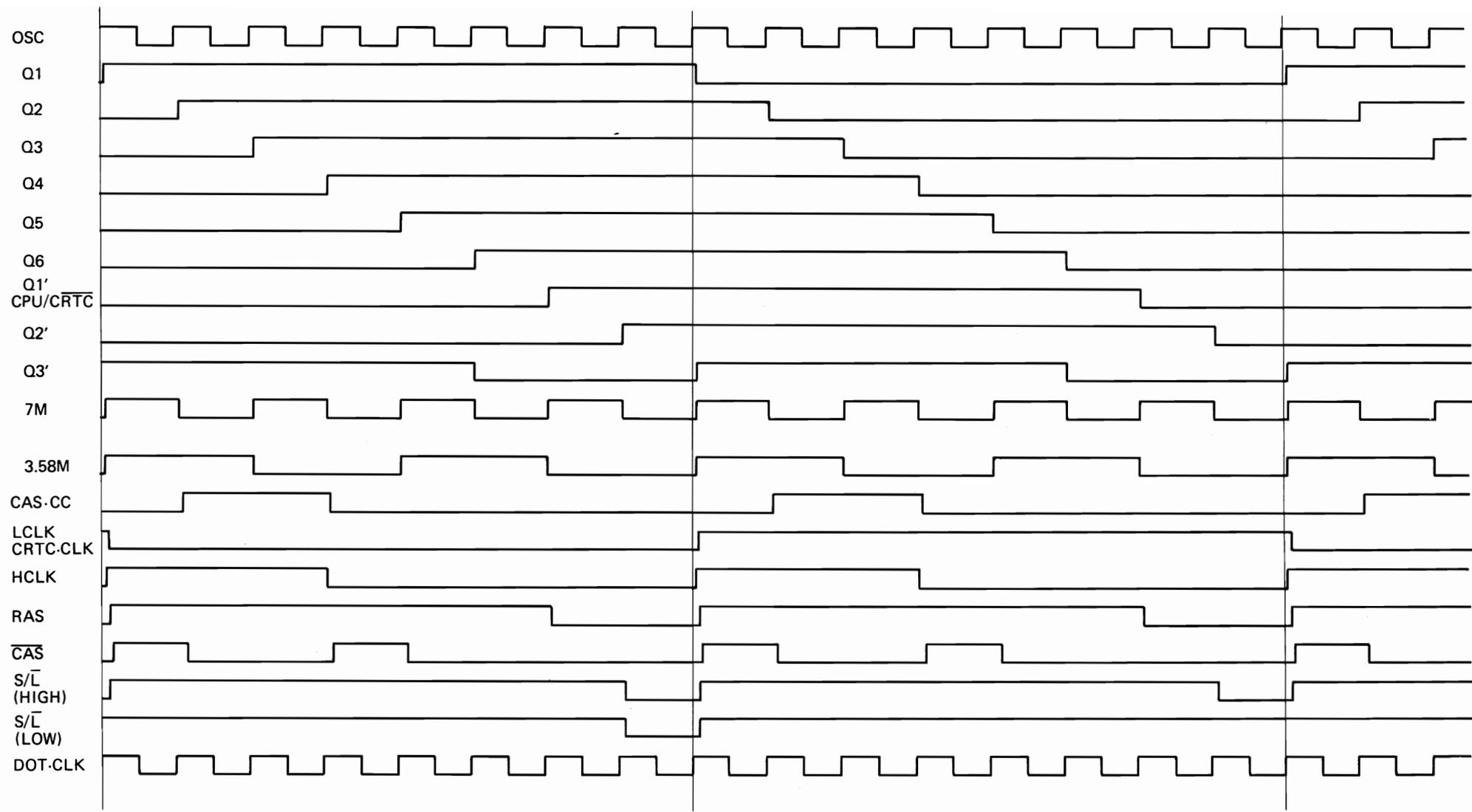
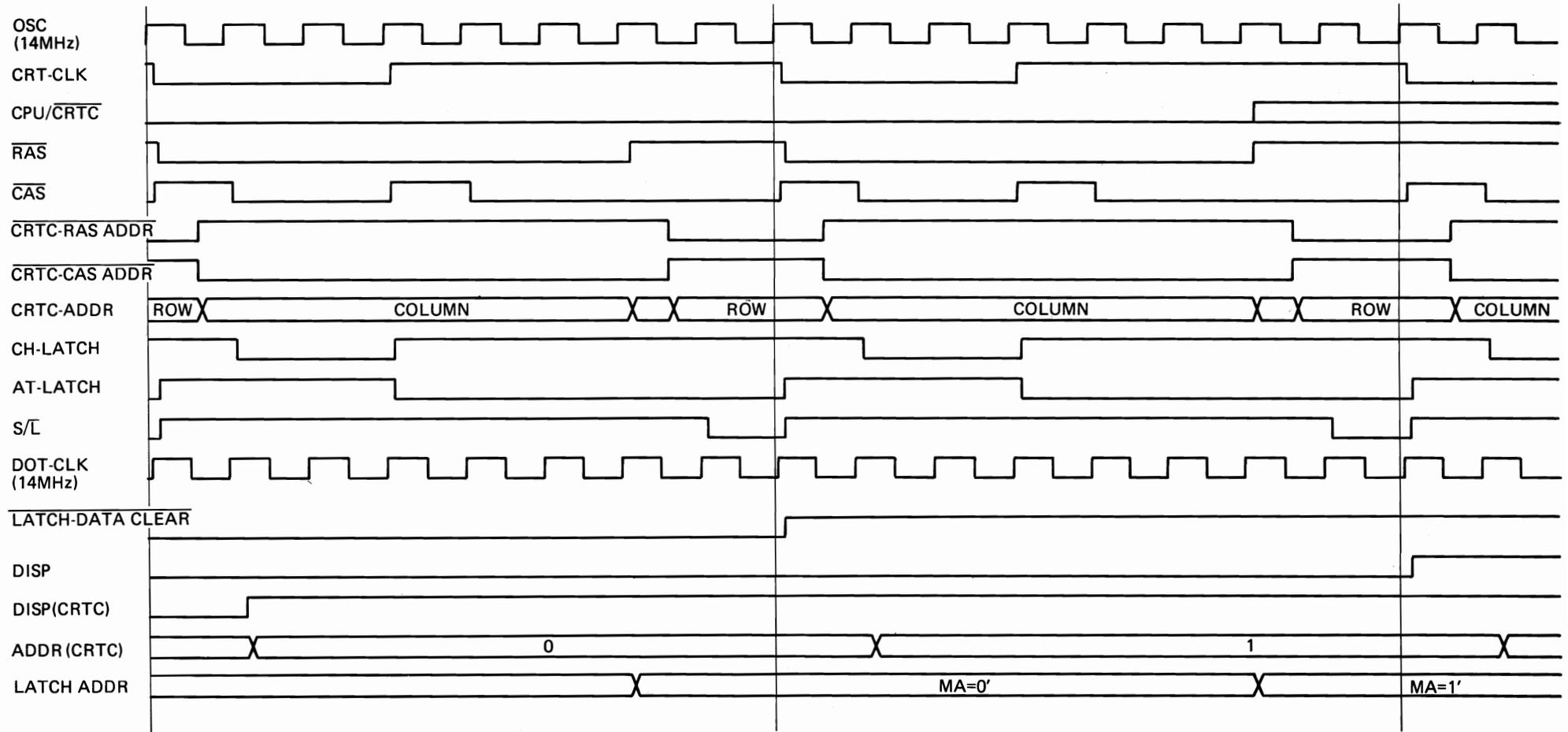


Figure 6-40



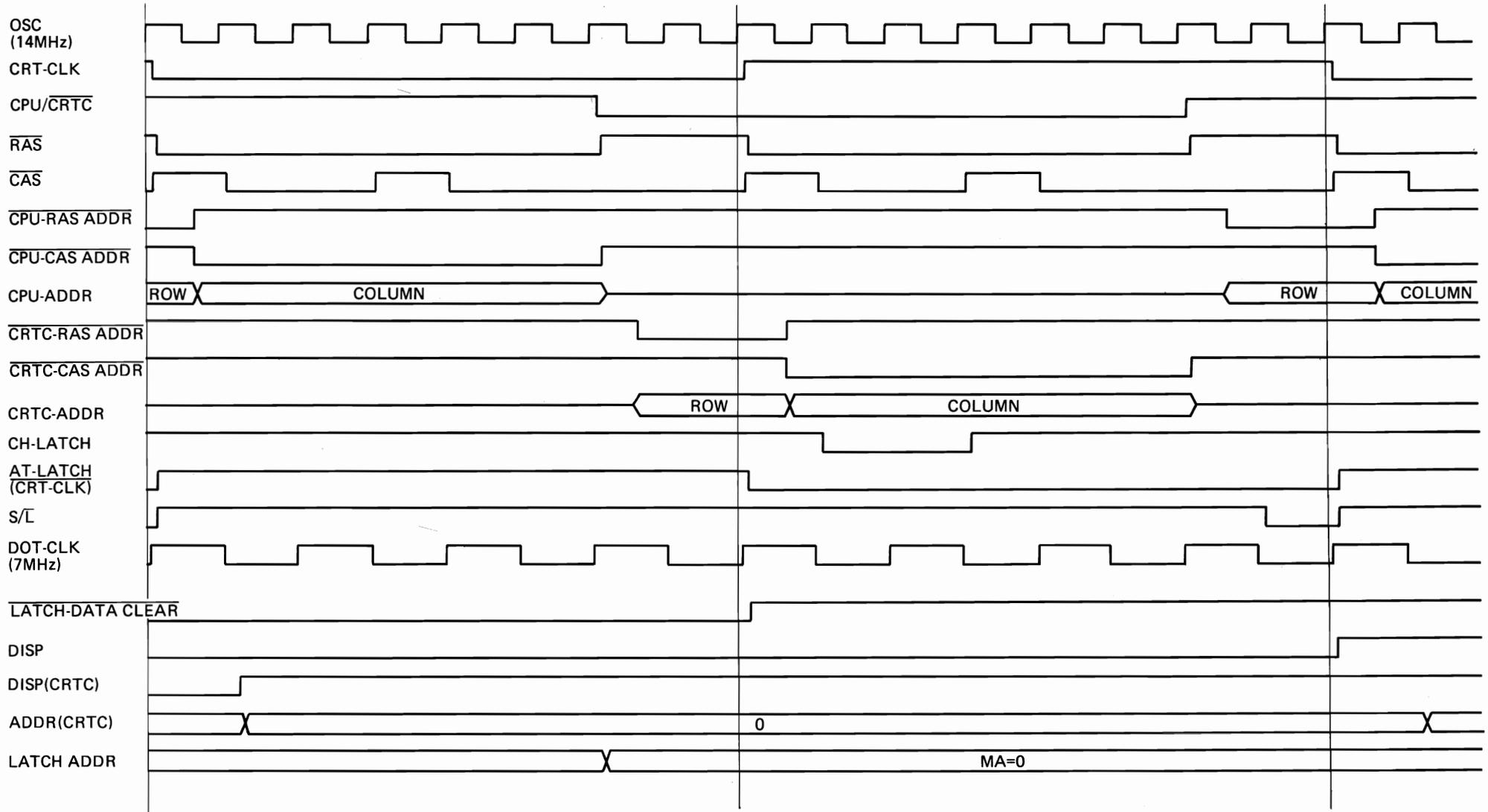
COLOR CRT CLOCK GENERATOR TIMING

Figure 6-41



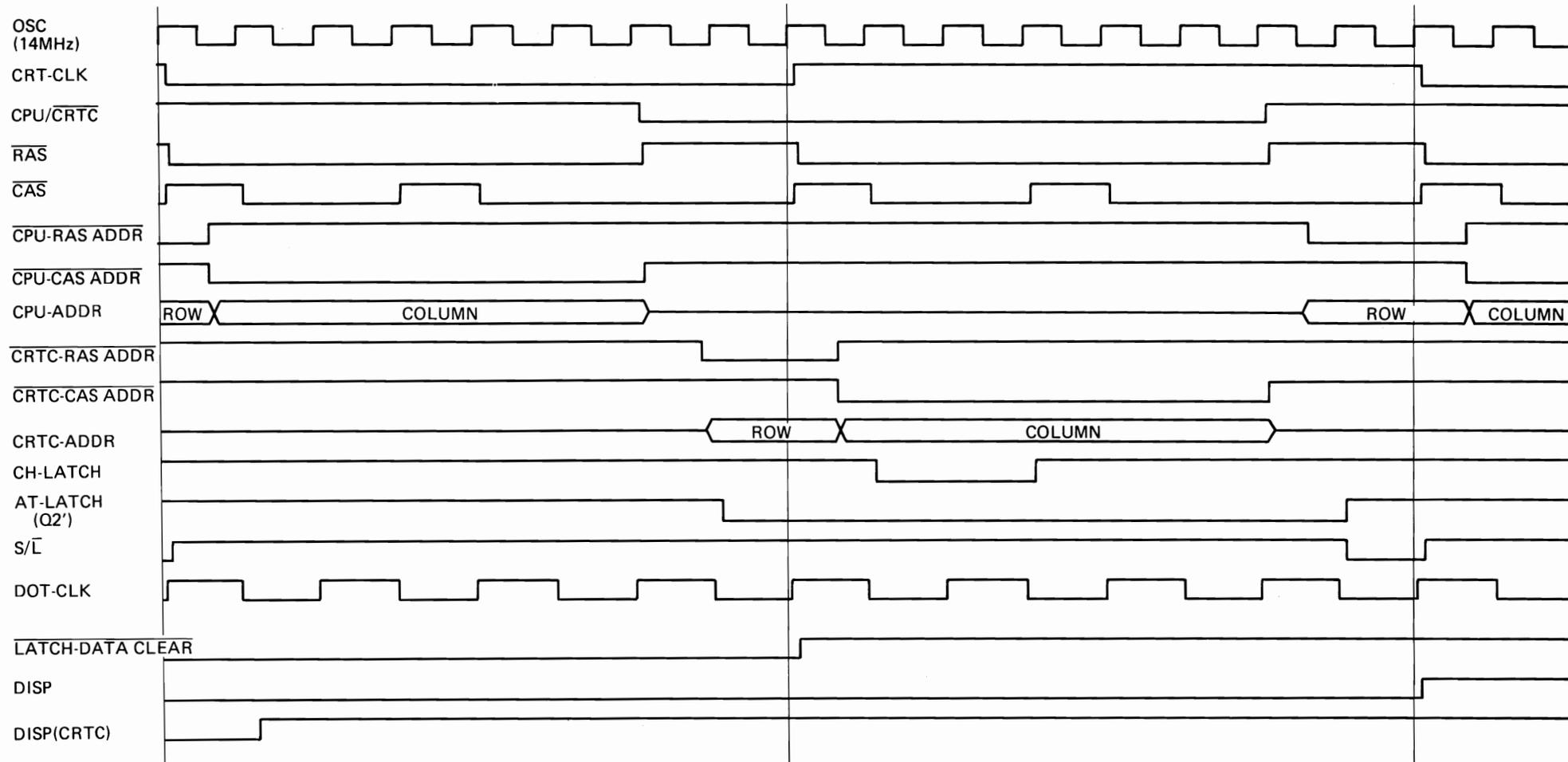
80 x 25 CHARACTERS TEXT MODE TIMING

Figure 6-42



40 x 25 CHARACTERS TEXT MODE TIMING

Figure 6-43



320 x 200, 640 x 200 GRAPHIC MODE TIMING

Figure 6-44

- **Video Output**

- **80 × 25 or 40 × 25 Characters Text Mode**

A data latched at the CH-LATCH and the AT-LATCH signals is divided into the ROM address and the attribute data.

At the moment when the ROM address is decided, a data is output from the character generator (2364). This data is input to the shift register (U25; LS166) together with the S/\bar{L} signal and shifted per one bit. This CH data is mixed with the AT data and then latched to output.

Note that the cycle of the fundamental clock signals (DOT-CLK, CH.LATCH, AT-LATCH, S/\bar{L}) are different in both display mode.

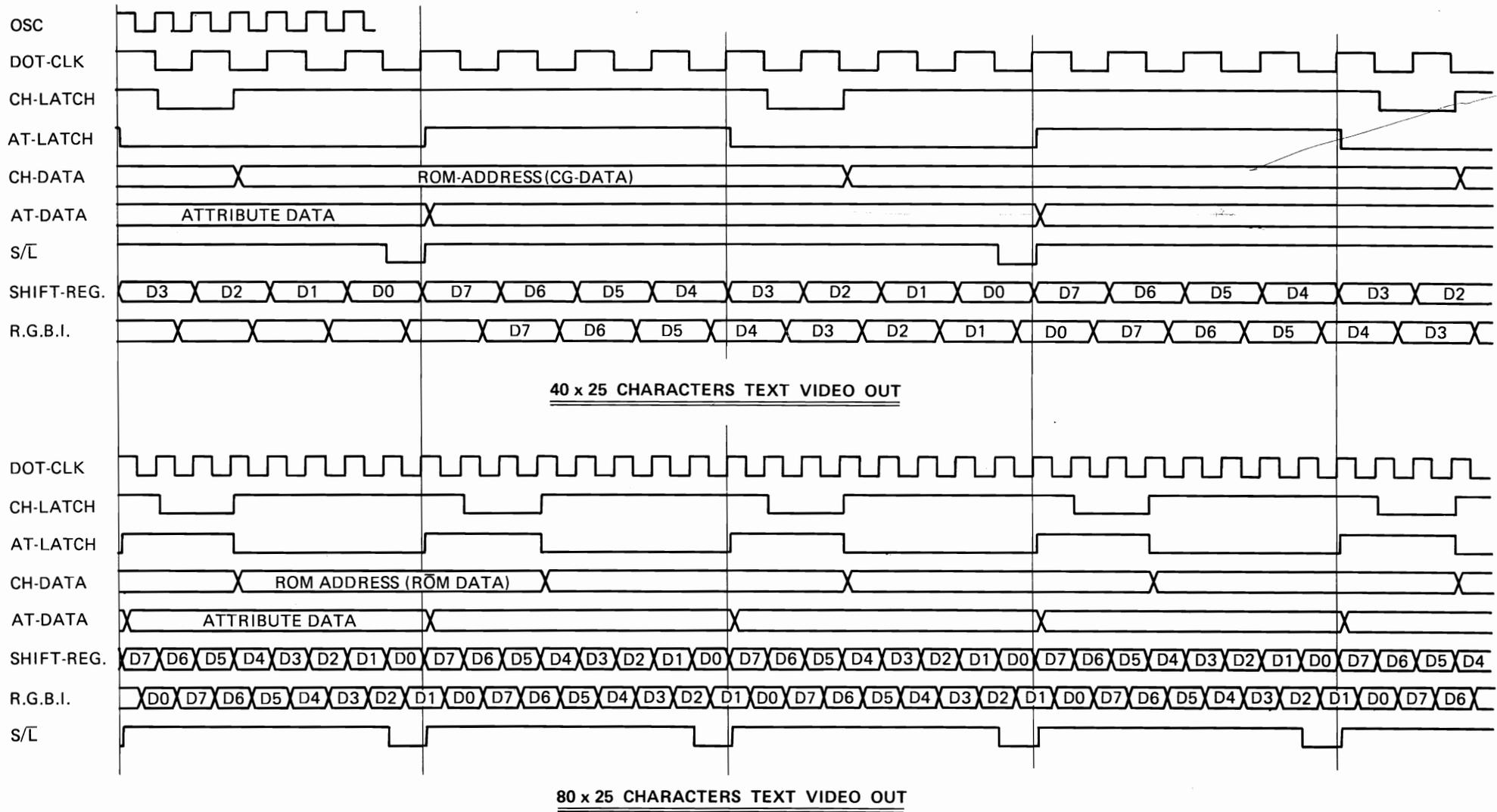


Figure 6-45

320 × 200 Pixels Graphics Mode

All dot data corresponding to the pixels on the CRT has 2 bits of information. Therefore, various colors can be displayed.

A data latched with the CH-LATCH and AT-LATCH signals is loaded at the U35 and U36 (LS166) and is shifted per one bit at the rising edge of the next clock cycle. This data is output synchronizing with the DOT-CLK signals after a color information is mixed to it.

As mentioned above, since one dot consists of 2 bits, four (2^2) colors can be displayed.

640 × 200 Pixels Graphics Mode

Basically, a method of displaying for this mode is identical to the 320 × 200 pixels mode. However, since every dot to be displayed corresponds to every bit, no color except black and white can be used.

Data outputs from the QH terminals of the U35 and U36 are output by enabling with the C1-EN and C0-EN signals at the U52.

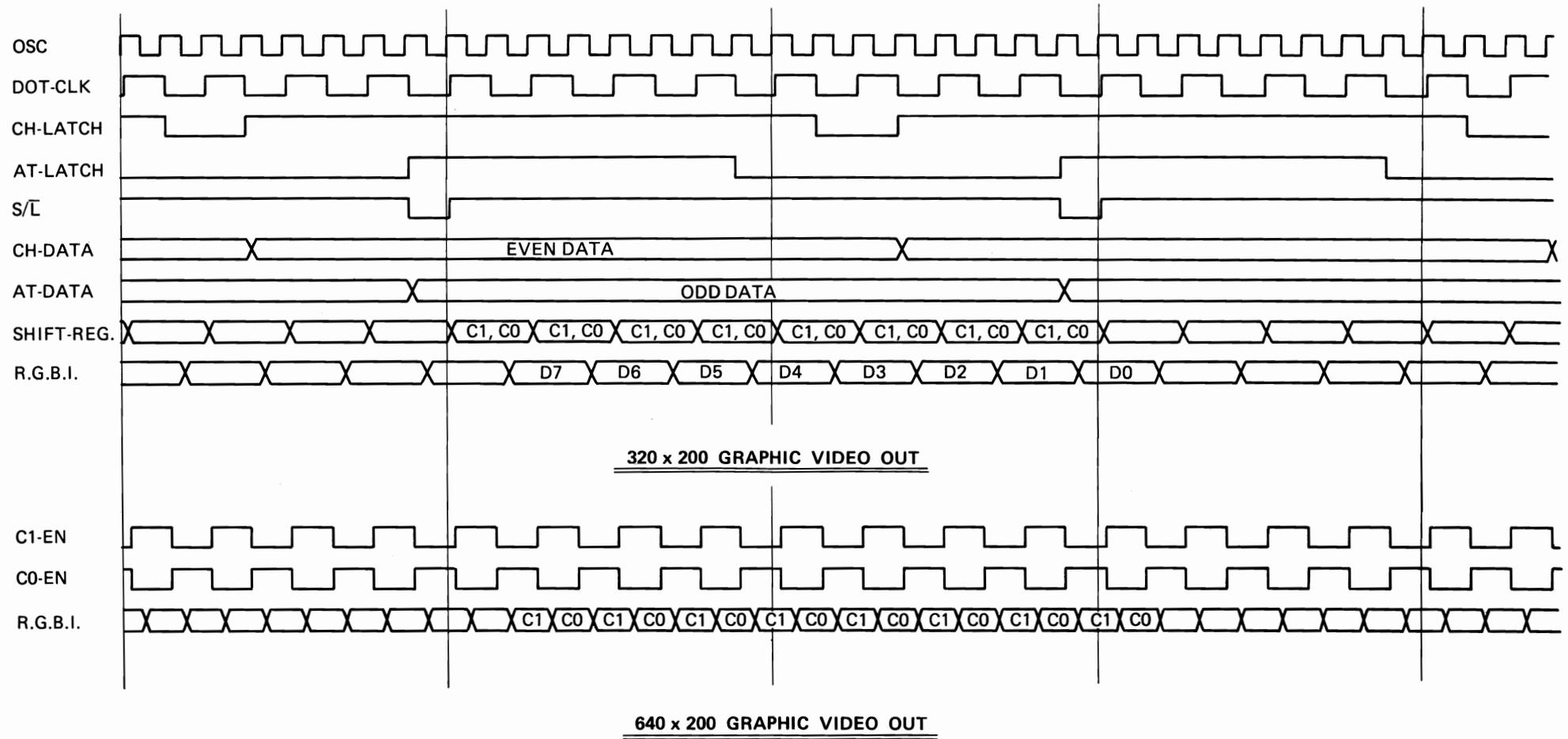


Figure 6-46

VI-5. Power Supply Unit

The 230V AC power sent through the AC inlet on the rear panel goes through fuse FS1, noise filter L1 then enters bridge diode D1. This AC power source is rectified and smoothed by D1, C6 and C7. Then this DC power is sent to the primary coil of oscillation transformer T1 via the transistor TR3. This transistor is controlled by IC1 on the sub printed board to regulate the +5V output voltage.

Triac TRK1 and resistor R2 protect the circuit against excessive current flow. When the AC power switch is turned on, a surge current is fed through resistor R2 and then TRK1 is turned on. Even if TRK1 does not operate, the internal thermal fuse of R2 is blown to protect the circuit.

IC1 (MPC494C) on the sub printed board controls TR3. At the first pin of this IC, it monitors +5 VDC output voltage which is obtained by photo-coupler PC2. IC1 then makes TR3 control the pulse width and frequency.

The +12 V power is generated by adding this +5 V and +7 V generated by D22 and C24. The +5 V power supply has a over voltage protection circuit which is controlled by photo coupler PC1. When an over voltage is detected, the photo coupler PC1 activates and then control voltage for IC1 on the sub printed board is cut off.

IC2 acts as an over current protector for the +5 V and +12 V power supply lines. This IC detects voltage drops at R53 and R52 which are inserted at the +5 V power supply line and at R51 for +12 V power supply line. If an excessive current greater than the specified value, IC1 reduces the pulse width of the signal to be sent to TR3 and as a result, the voltage of the +5 V line drops.

This power supply also has a protection circuit against short circuiting of the output. Thermostat TH1 is mounted on the heatsinker together with D21, and when the temperature of the heatsinker reaches to 95 degrees centigrade, photo coupler PC1 activates, and finally, internal oscillation of the IC1 stops.

The -12 V voltage is regulated by the three-terminal voltage regulator IC1 and another control voltage for IC1 on the sub printed board is regulated by TR1 and ZD1 on the sub printed board.

PART VII

DIAGNOSTIC PROGRAMS

CONTENTS

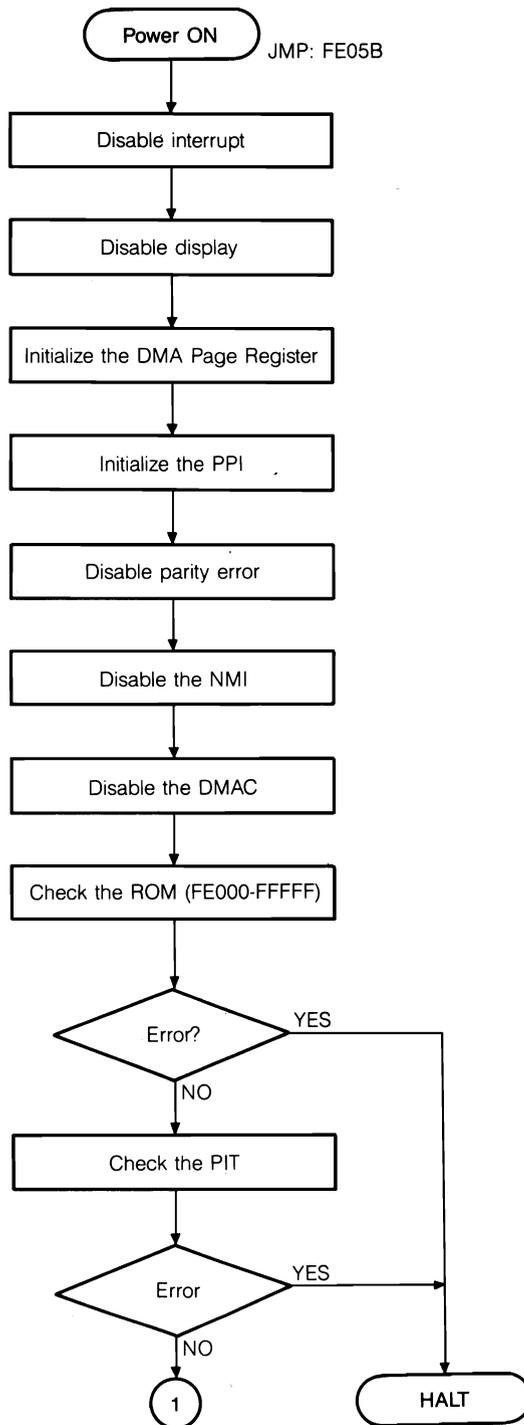
Diagnostic Programs	118
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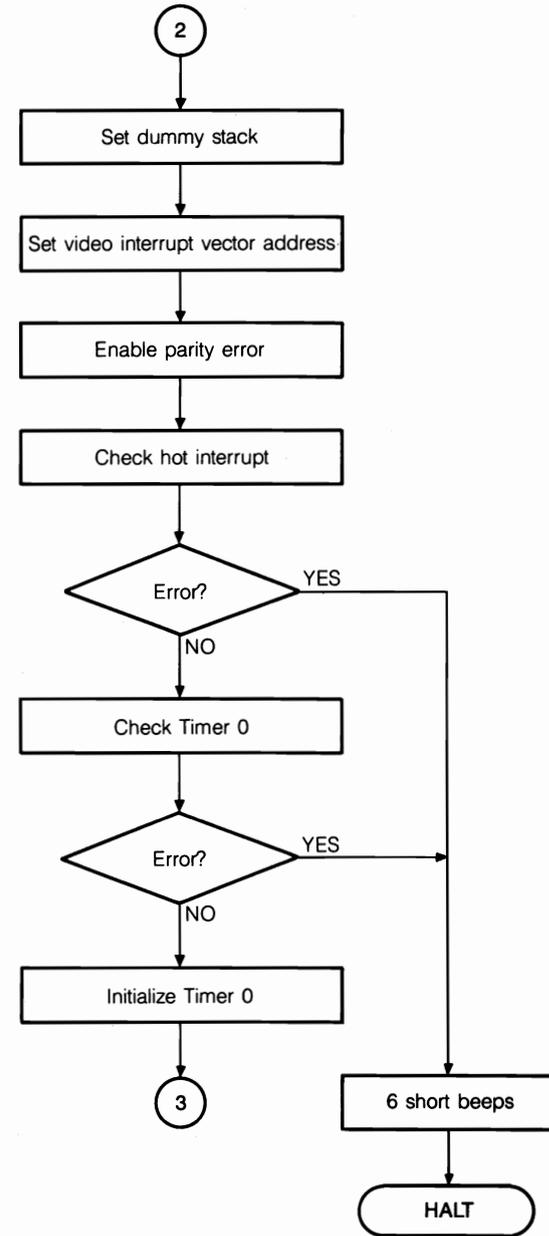
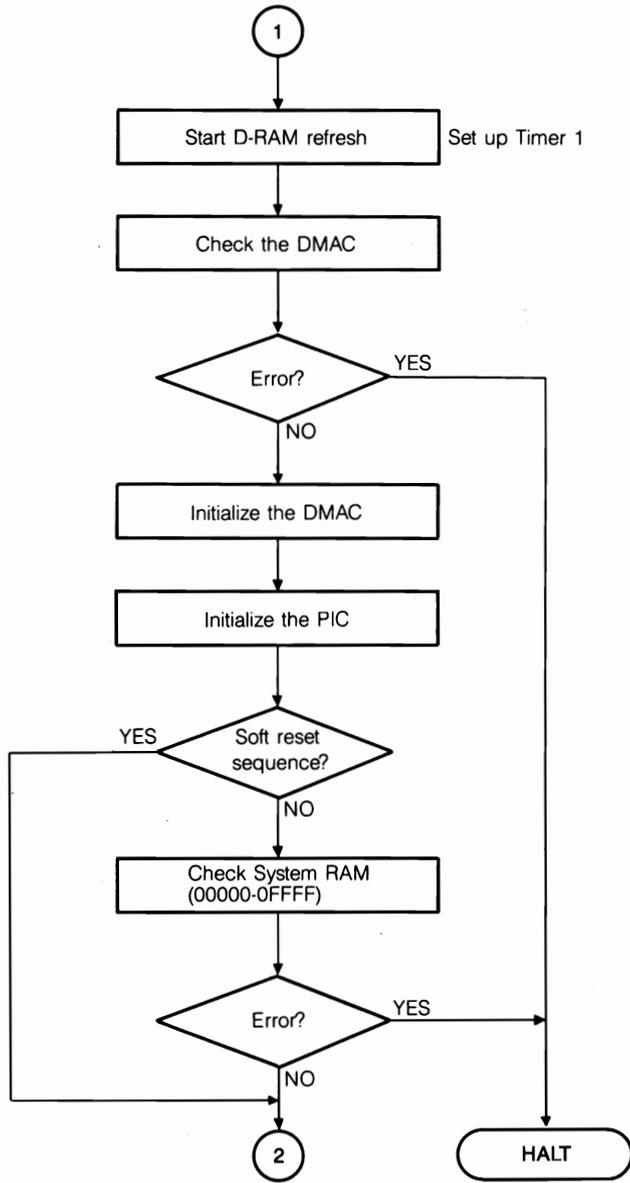
Diagnostic Programs

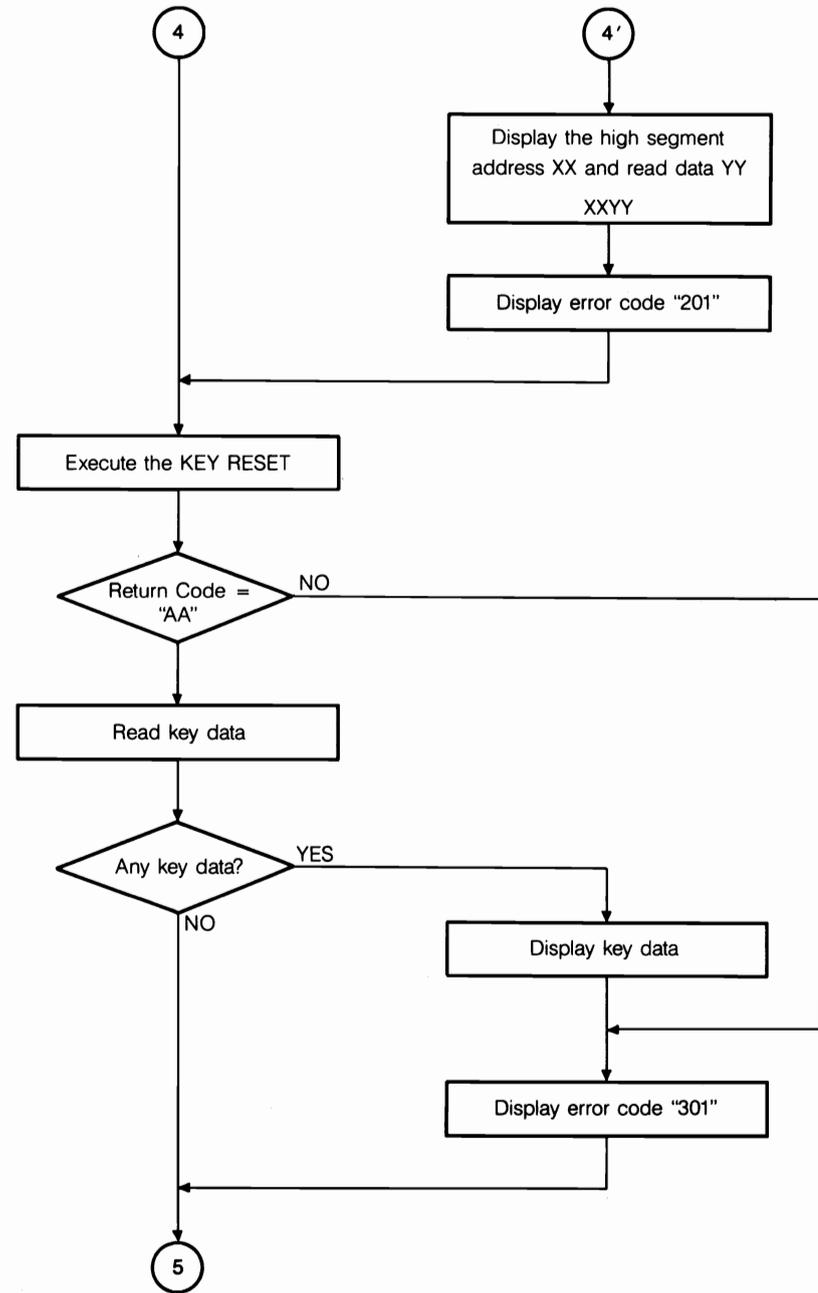
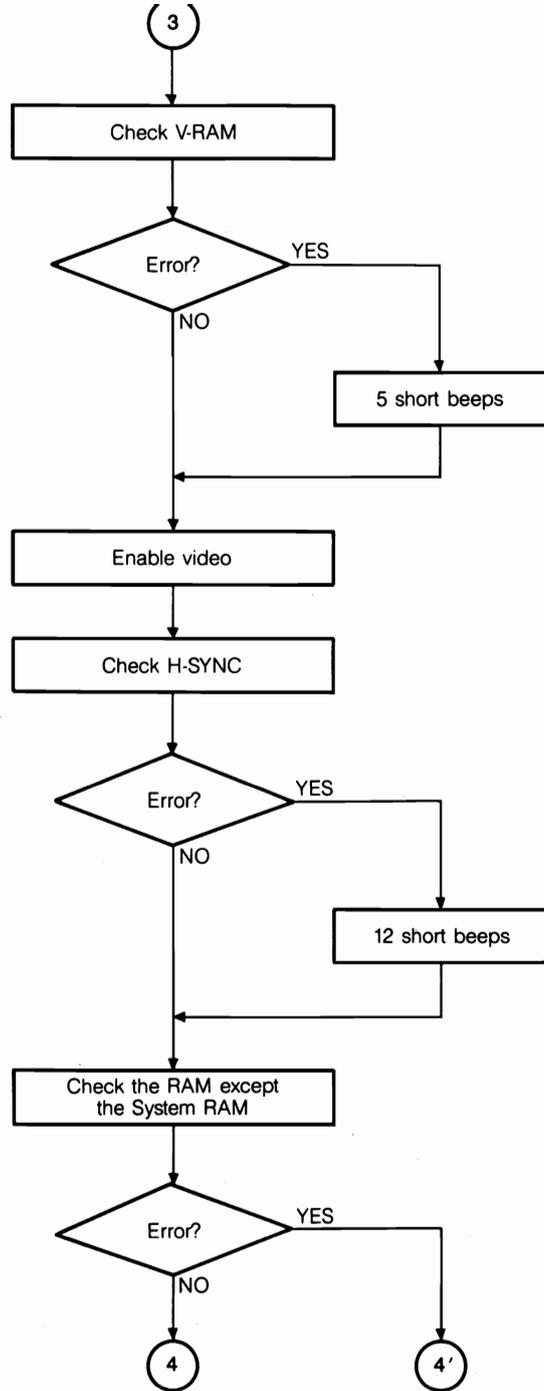
In order to check the computer and peripherals effectively and quickly, the A-200 has two diagnostic programs as standard software. One is ROM-based power-on diagnostics and the other is contained in the supplied disk.

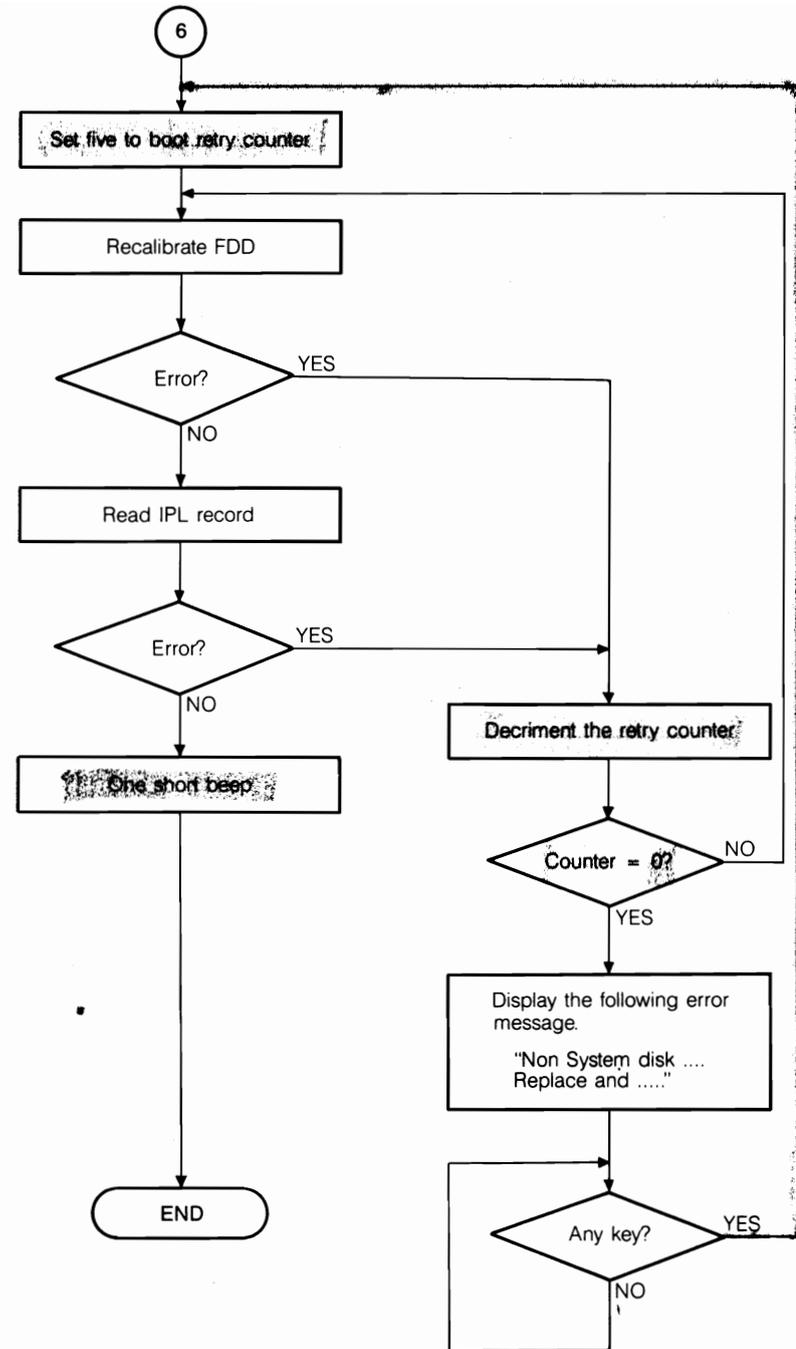
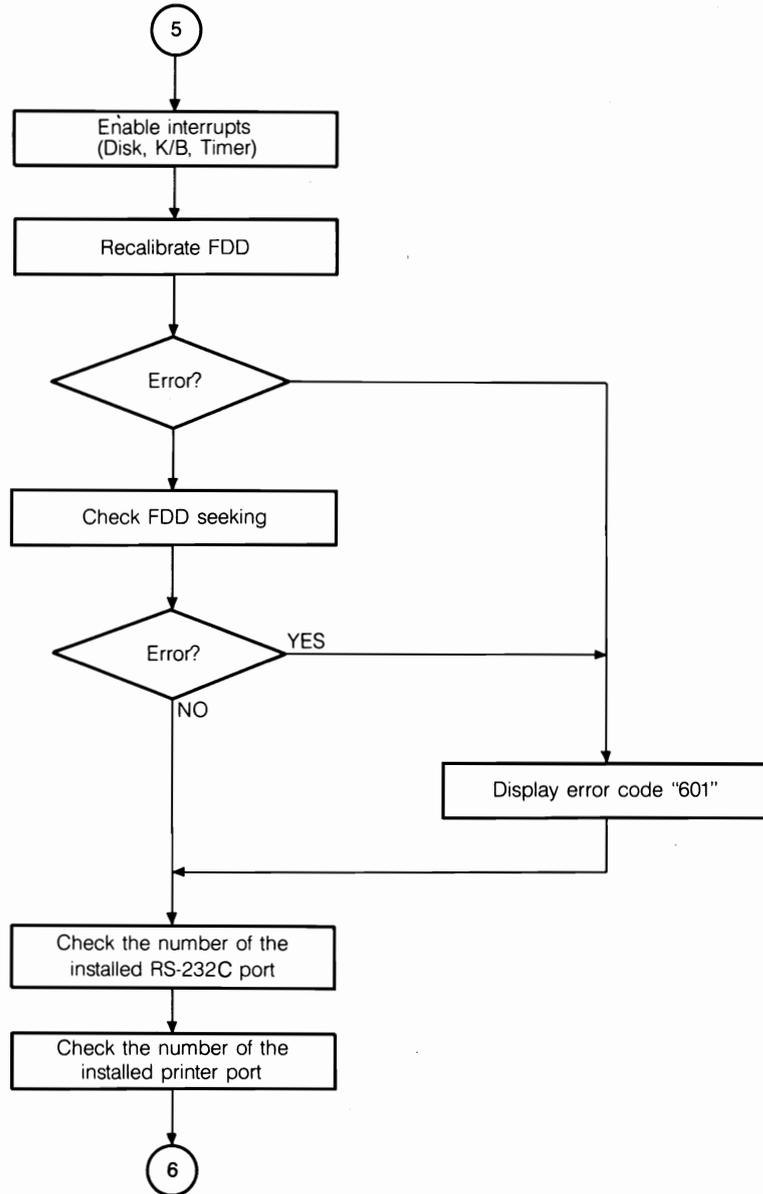
ROM-based power-on diagnostics

This test program is contained into the built-in ROM and whenever a customer turns the computer on or the RESET button is pressed, the computer will perform this test automatically. The test program checks such devices or functions as ROM, RAM, keyboard, timer and video. Following is a detailed flow chart of this test.









Stand-alone diagnostic program

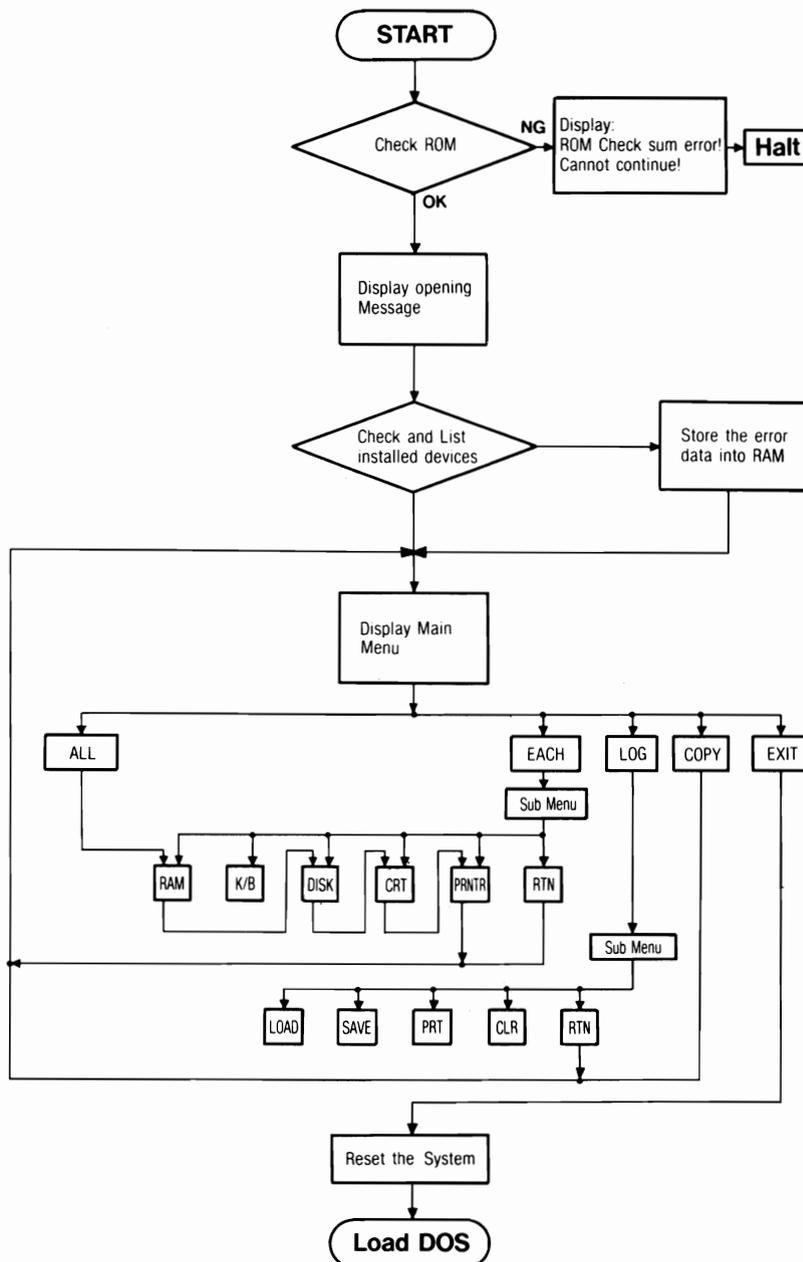
Since this stand-alone program is not controlled by the DOS, you cannot execute it by any of DOS commands. To start-up the program, first remove the DOS disk (System Disk I) or any other disk from the drive (if inserted) and then press the RESET button on the front panel of the computer, or turn the power of the computer off and then turn on again. Next, insert the Diagnostic disk into the drive A, and the computer will begin to load this program automatically. Then the following message will appear:

Canon Personal Computer DIAGNOSTIC
(C) Copyright Canon Inc. 1984, Ver 1.0

Press any key to start

Once this message appears, it is indicated that the whole contents in the disk have been transferred into the internal RAM. So in order to prevent the disk from accidental destroying, you should remove it from the drive.

The following is a general flow chart of this program.



Description of the Program

When the data stored in the disk has been transferred into RAM, the computer begins the internal ROM check. If any malfunction is detected, the following message will appear:

ROM check sum error ! Cannot continue !

then the computer will "halt", and give no further information to you. When this check is completed successfully, the message:

**Canon Personal Computer DIAGNOSTIC
(C) Copyright Canon Inc. 1984, Ver 1.0
Press any key to start**

will appear on the screen.

Pressing any key allows you to change the information on the screen and then the computer asks the configuration of the computer under test like:

SYSTEM CONFIGURATION

System board
Color/graphics adapter
2 disk drive(s) 256 KB memory

If OK press [Y]
if not press [N]

If these items fit your computer actually, press Y key and then the screen will change its indication to Menu. Or, if not, press N key. The A-200 will store the data temporarily into RAM and also returns to Menu.

**MAIN MENU
1-AUTO CHECK
2-EACH CHECK
3-LOG
4-COPY
5-EXIT DIAGNOSTIC**

Select the number in this menu.

1-AUTO CHECK: When you choose this item, following test will be executed sequentially.

- * RAM R/W check
- * Disk R/W check
- * Display monitor check
- * Printer check
- * Returns to MAIN MENU

First, the following message will appear:

PREPARATION OF AUTO CHECK

Insert scratch disk(s) in drive A (and B) for disk check.

Press any key to start.

Insert one or two formatted disk(s) into the drive(s), and press any key to start up this program. The messages for each check point will be displayed sequentially. For detailed description concerning each check point, refer below.

2-EACH CHECK: Entering this selection allows you to display EACH CHECK MENU on the screen. In this mode, you can check any of each items as indicated below:

EACH CHECK MENU

- 0-RAM R/W CHECK
- 1-KEYBOARD CHECK
- 2-DISK R/W CHECK
- 2-CRT CHECK
- 4-PRINTER CHECK
- 5-RETURN TO MAIN MENU

Select the number in this menu.

• **RAM R/W TEST**

Description: The computer writes one word data to the specified RAM area and then reads it. If the read data is the same as the written data, the computer changes the pattern of one word data. the patterns of one word data are FFFF, AA55 and 55AA. The specified RAM area is 03500 to the address determined by the DIP switch on the main P.C.B.

Error Message: If an error occurs, following message will appear:

segment — XXXX (Number of address where an error was occurred.)
offset — YYYY (Number of address where an error was occurred.)
write data — ZZZZ (Previously written data)
read data — WWWW (Read data)

Press any key to exit.

When this check is completed successfully, the message:

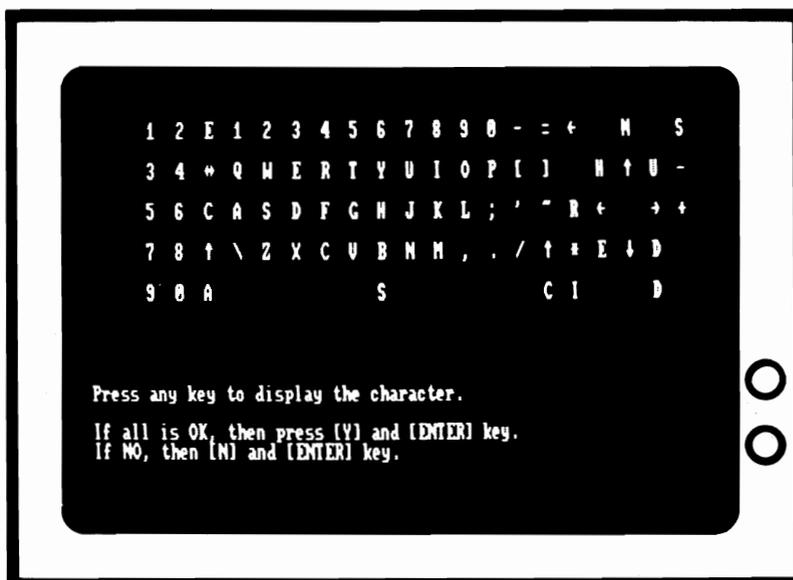
Memory read/write check OK !

Press any key to exit.

To exit this test: Pressing any key returns the screen to EACH CHECK Menu.

• **KEYBOARD CHECK**

Description: As shown in the figure below, the configuration of the keyboard consisted of a squares on the screen. These squares will changes to the respective characters as you press each key.



Error Message: None. However, if displayed character is different from one you have just keyed in, press "N" key and then ENTER key. The following message will appear:

Keyboard is not normal
Press any key to exit this check.

Pressing any key allows this test to return to EACH CHECK menu.

To exit this test: Press "Y" key and then ENTER key.

• **DISK R/W CHECK**

Description: The computer writes the specified data (D6B6) onto all tracks on a disk and then reads them. The written and read data will be compared. Before executing this program, be sure to insert one or two disk(s) into the drive(s). Note that this program destroys the contents of the disk(s). So you should not use the disk(s) which contains important data or programs.

Press [A] key to check drive A
Press [B] key to check drive B
Press [ESC] key to exit

will appear. Press appropriate key in response to above prompt.

Error Message:

Disk R/W error !
WXYYZ

Press any key to return

where W is a drive number, X is a head number, YY is a track number and Z is a sector number.

To exit this test: After the prompt below, press any key then ESC key. The test will return to EACH CHECK Menu.

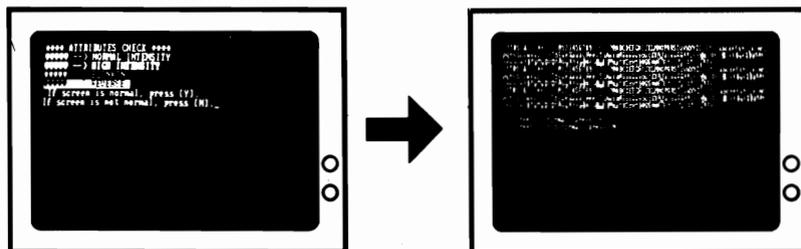
Drive check OK !

Press any key to return

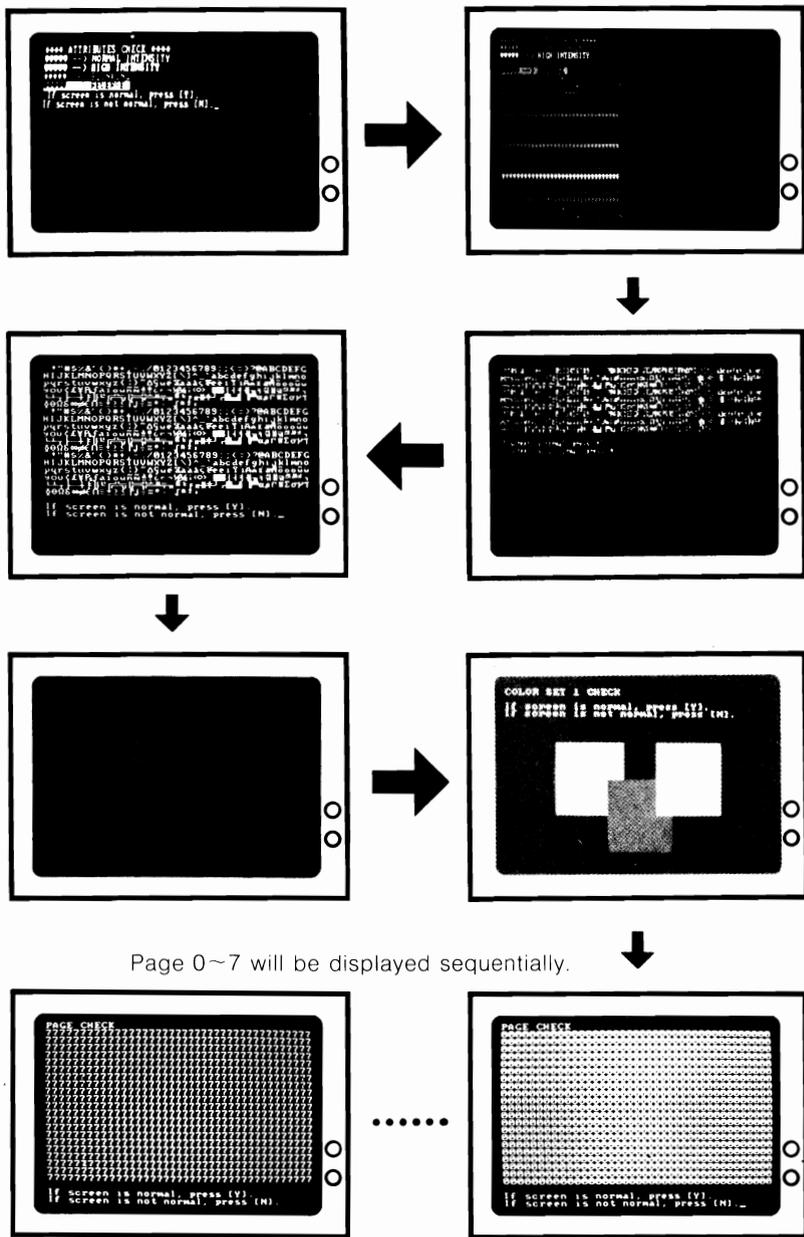
• **CRT Check**

Description: Various patterns of display will be indicated on the display monitor. The computer asks you identities of information at every screen. This test is divided into some sections according to the type of display adapter board. Following illustrations show the information to be displayed. If your A-200 is a monochrome display version, another items than an attribute check and 80 x 25 character set check will not be performed.

Monochrome Version



Color Version



Error Message: None. You should check the information displayed on the screen with your eyes by referring to the illustrations above.

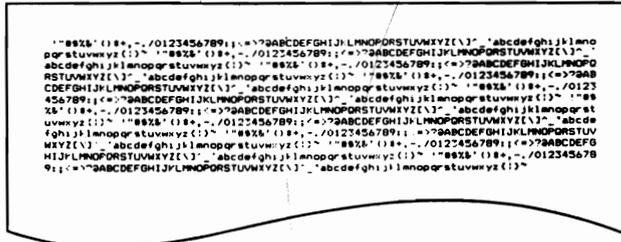
To exit this test: When you enter Yes or No in response to the question displayed on the last screen, the test will return to EACH CHECK Menu.

• **PRINTER CHECK**

Description: This test makes a printer to print out following characters. If any malfunction is found at the printer interface, an error message will be displayed. However, you should check a difference between printed characters and following illustration. When this check is selected, the following message:

Printer check
Press any key to start printing

is displayed. Insert a paper into your printer and press any key to start this check.



Error Message: If an error at the interface is detected, one of the following messages will appear after the prompt "TIME OUT ERROR":

- Echo back check error
- I/O error
- Printer is not selected
- Out of paper
- Acknowledge is not received

To exit this test: When it is found that the printer is normal, following message will appear. Pressing any key allows the test to EACH TEST Menu.

Printer check is OK !
Press any key to exit

3-LOG

A submenu will displayed when you select this item.

To check the error that occurred in some test, select number in following menu.

- 1-LOAD (loads error data and displays error list)
- 2-SAVE (saves error list on memory to disk)
- 3-PRINT out LOG list
- 4-CLEAR LOG list
- 5-RETURN to main menu

• **LOAD**

An error data stored in the disk will be written onto the RAM of the A-200 and then it is displayed on the screen. In this case, another error data previously stored in the RAM will be erased.

- **SAVE**

All errors occurred during a series of Diagnostic program have been recorded into the RAM of the computer as data. That data will be written onto the head 0, track 04 and sector 1 of drive A by selecting this command. Therefore, if the write protect notch on Diagnostic Program disk is covered with a tab, be sure to remove it before executing this command. You can also save the error data onto other disk which has been formatted by executing the FORMAT command provided in the DOS.

- **PRINT out LOG list**

An error data currently stored on the RAM will be printed out to a printer. If the printer is not connected, following message will appear after a few seconds:

Printer is not connected. Press any key.

When any key is pressed, the error data currently stored in the RAM is displayed on the screen. When listing on the screen is finished, pressing any key allows the program to return to the main menu.

- **CLEAR LOG list**

This command clears all error data stored on the RAM and on the disk currently in use.

- **RETURN to main menu**

Select this command to return to Main menu.

4-COPY

The information stored into Diagnostic Program disk cannot be copied onto another one with the DISKCOPY command provided in the DOS, because this Diagnostic Program is not controlled by the DOS. Use this COPY command in making a back-up copy.

Following message will appear on the screen:

**Insert DIAGNOSTIC PROGRAM disk in drive A.
Press [ENTER] key to start loading.
Press [ESC] key to exit.**

Insert Diagnostic Program disk into the drive A and press ENTER key. When the information stored on the disk is transferred onto the internal RAM, a message:

**Loading completed
Insert target disk in drive A.**

**Press [ENTER] key to start copying.
Press [ESC] key to exit.**

will appear.

Remove Diagnostic Program disk from the drive A and insert a formatted disk instead, and then press ENTER key.

When the copy is completed a message:

Copy completed !

Press [ENTER] key to return to main menu.

will appear.

5-EXIT DIAGNOSTIC

Use this command to exit this diagnostic program and return to DOS mode. A message:

Insert system disk in drive A.

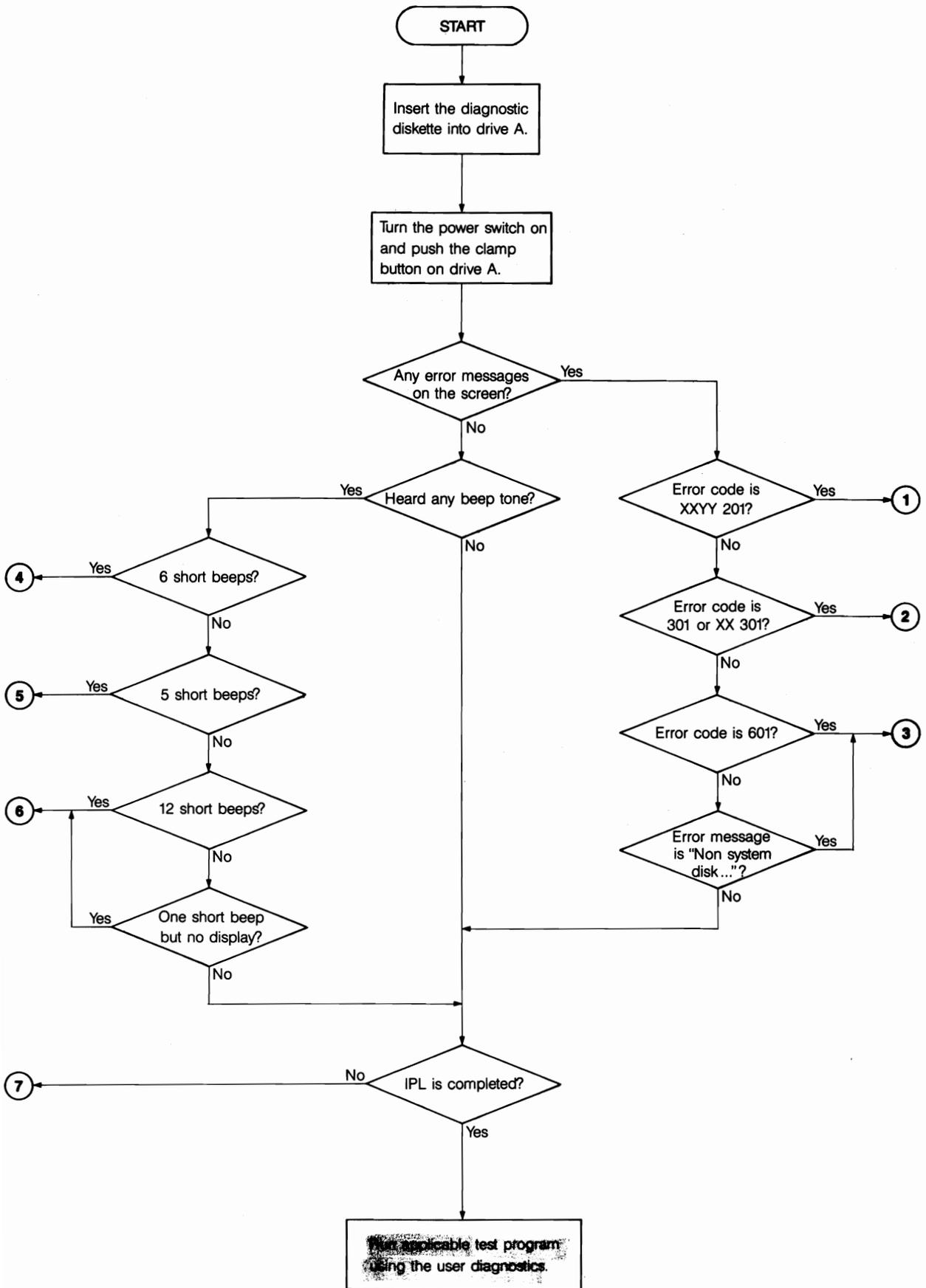
Press any key to get ready.

will be displayed. Remove Diagnostic Program disk and insert the DOS disk instead, and then press any key. The computer will begin to boot the DOS disk.

PART VIII

TROUBLESHOOTING

Troubleshooting



① RAM failure except the system RAM area

The read data and written data don't match in the address 10000-3FFFF and 40000-7FFFF. The patterns of data are "AA, 55, 00 and FF".

XX denotes the segment address where the error has occurred and YY is the actual data read from the RAM.

* If the error bit is only one bit such as "01" or "FE", replace the RAM chip in accordance with the following table.

Error Bit		D8 or D0	D9 or D1	D10 or D2	D11 or D3	D12 or D4	D13 or D5	D14 or D6	D15 or D7	Parity
Segment	00-0F	Not checked in this test								
Main PCB	10-1F	U36 or U37	U31 or U32	U26 or U27	U22 or U23	U18 or U19	U13 or U14	U9 or U10	U5 or U6	U1 or U2
	20-3F	U38 or U39	U33 or U34	U28 or U29	U24 or U25	U20 or U21	U15 or U16	U11 or U12	U7 or U8	U3 or U4
Optional RAM Board *	40-5F	U2 or U11	U3 or U12	U4 or U13	U5 or U14	U6 or U15	U7 or U16	U8 or U17	U9 or U18	U10 or U19
	60-7F	U21 or U30	U22 or U31	U23 or U32	U24 or U33	U25 or U34	U26 or U35	U27 or U36	U28 or U37	U29 or U38

* When S1-1 and S1-5 are on.

Table 8-1

* In other case, check the interface signals.

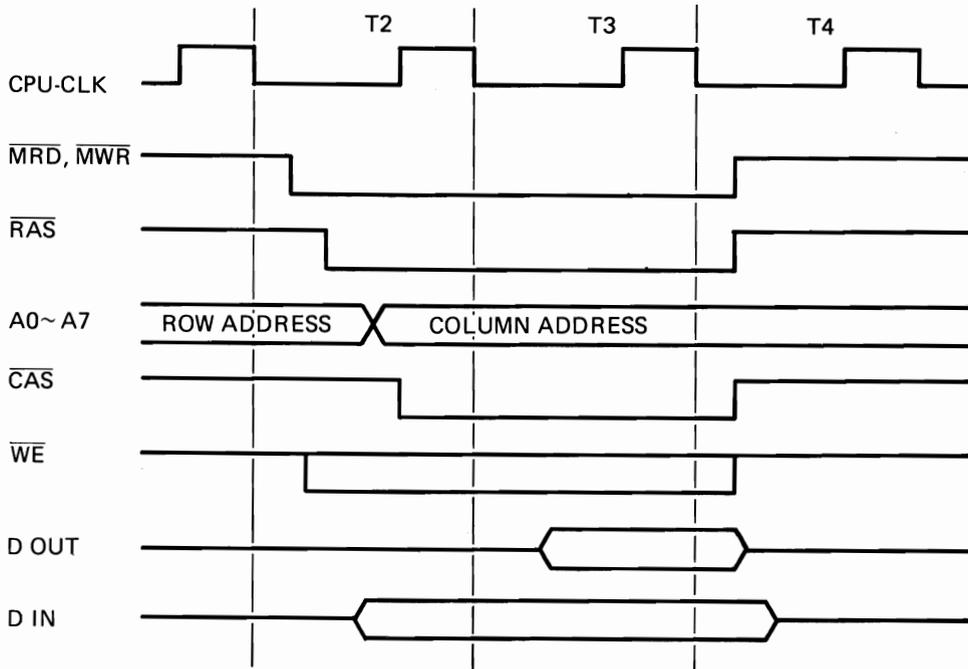


Figure 8-1

② Keyboard failure

* XX 301

XX is the key code whose key switch is always on, refer to Table 6-11 and replace it.

* 301

Key Reset is not completed.

Check the PPI (CS, A0, A1, RD, WR, and D0—D7 signals).

Check the interface signals.

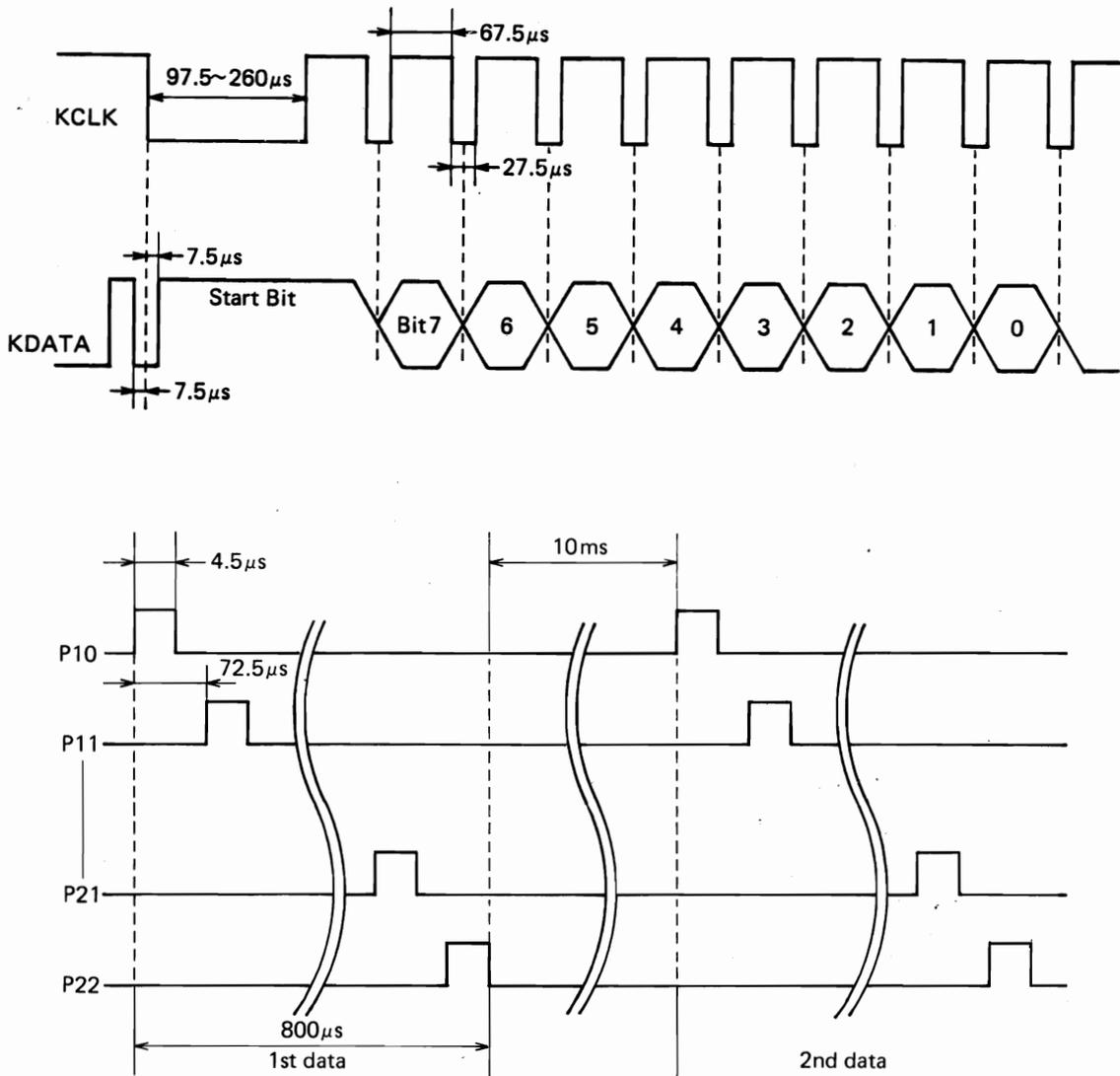


Figure 8-2

③ FDD or FDC failure

- * Check the cable from the power supply.
- * Check the cable from the main PCB.
- * Check the timing clock generator circuit.

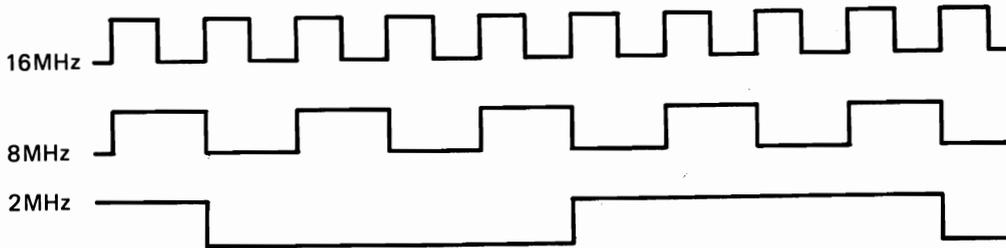


Figure 8-3

- * Check the VFO circuit.

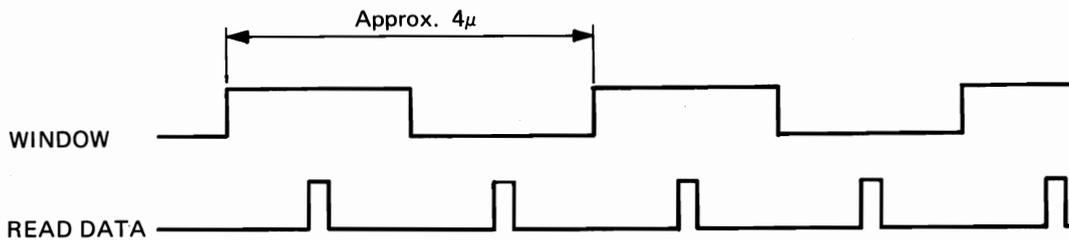


Figure 8-4

- * Check the signals shown below.

INDEX	Pin 17 of FDC	SIDE	Pin 27 of FDC
TRK0	Pin 33 of FDC	WG	Pin 25 of FDC
<u>DRIVE 0</u>	Pin 8 of U132	DIR	Pin 38 of FDC
DRIVE 1	Pin 6 of U132	STEP	Pin 37 of FDC

④ PIT or PIC failure

An unexpected interrupt has been received during the interrupt mask register of PIC is reset, or the timer 0 clock is too early or too late.

- * Check IRQ0—7 and INT signals.
- * Check PCLK, CLK0, CLK1 and CLK2 signals.

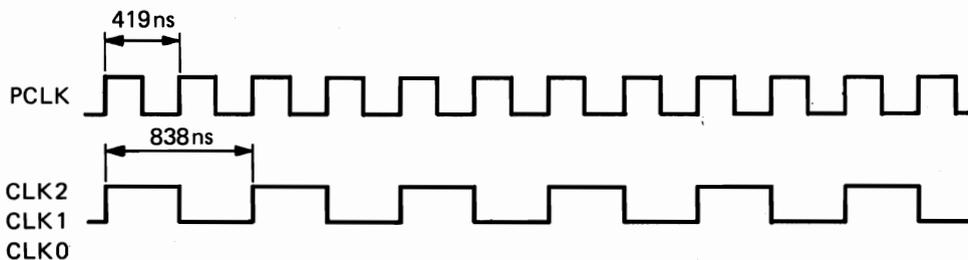


Figure 8-5

⑤ V-RAM failure

The read data and written data don't match in the V-RAM area. The patterns of the data are "AA, 55, 00 and FF".

To determine the error bit, run the CRT check in the diagnostic program.

⑤-1. Monochrome Board

* If the error bit is in even address, the displayed character may be different and if the error bit is in odd address the displayed attribution may be different.

Replace the V-RAM chip in accordance with the following figure.

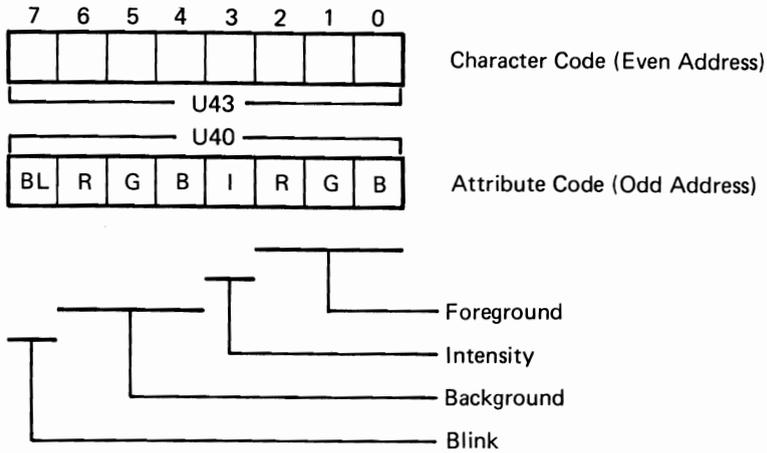


Figure 8-6

⑤-2. Color Board

* Check for lower 4K-byte of V-RAM

Using the 80 x 25 characters text mode, determine the error bit. If the error bit is in even address, the displayed character may be different and if the error bit is in odd address, the displayed attribution or color may be different.

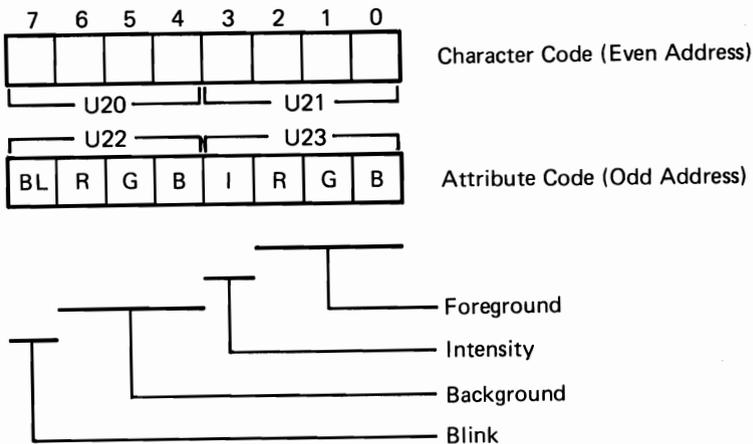


Figure 8-7

* Check for the 16K-byte V-RAM

Using the 320 x 200 pixels graphic mode, determine the error chip.

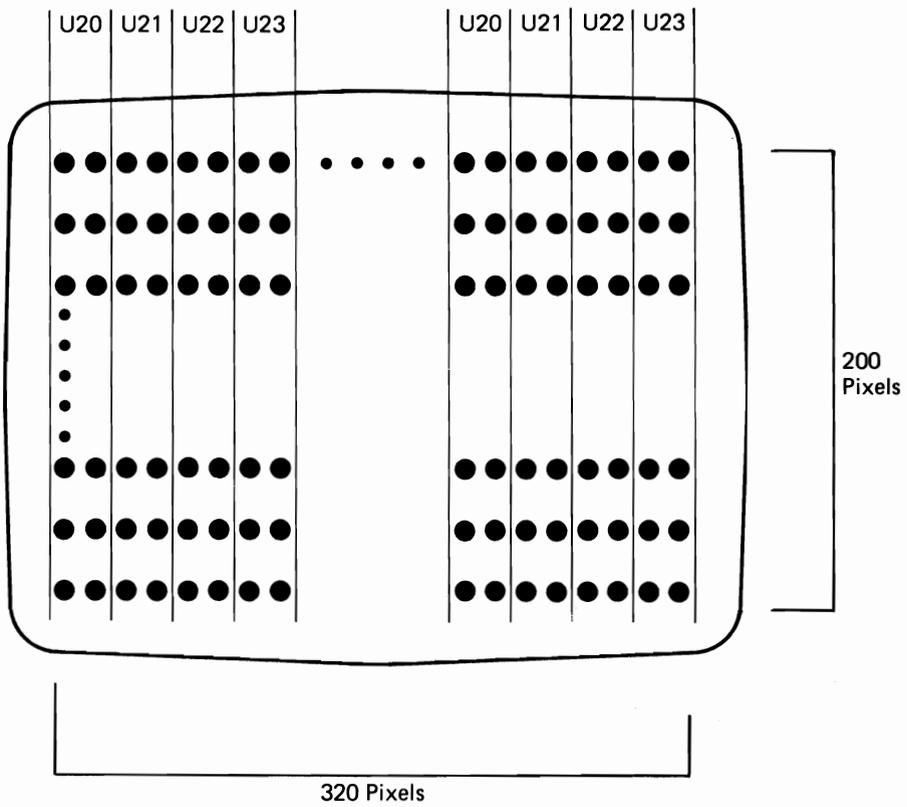
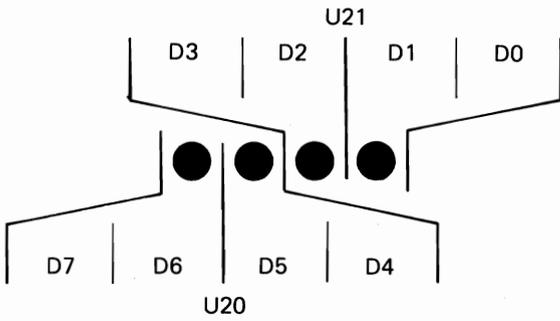


Figure 8-8

⑥ H-SYNC failure

Could not detect the H-SYNC signal.

⑥-1. Monochrome Board

* Check the H-SYNC signal.

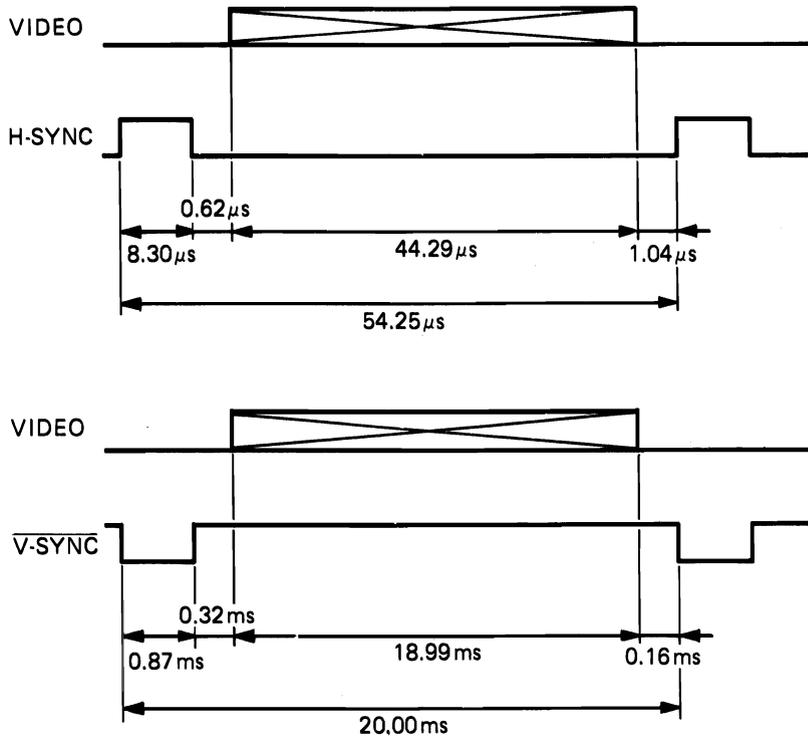


Figure 8-9

* Check the clock generator circuit.

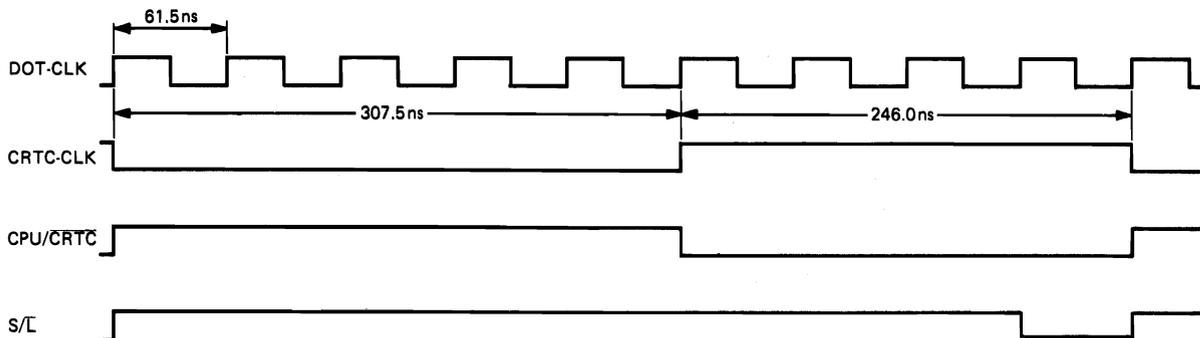


Figure 8-10

⑥-2. Color Board

* Check the H-SYNC signal.

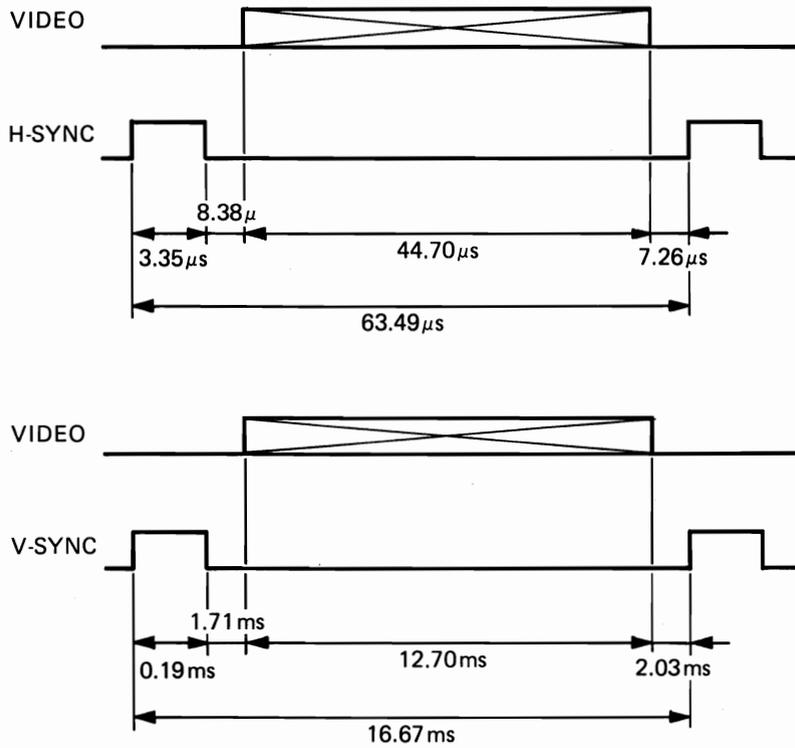


Figure 8-11

* Check the clock generator circuit.

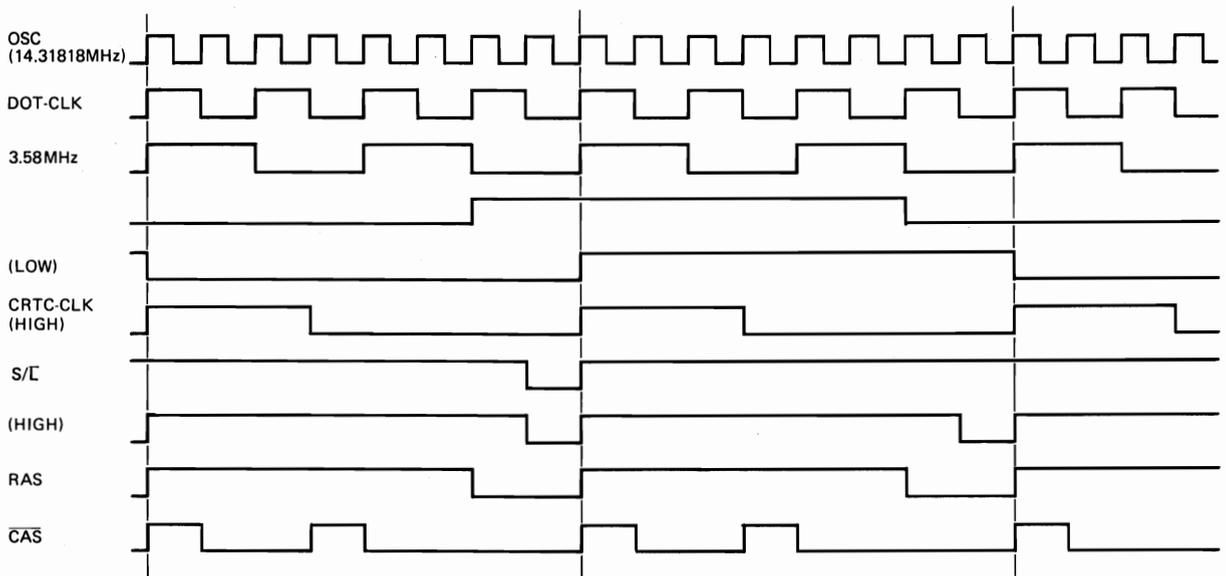


Figure 8-12

⑦ Basic function failure

* Check the power supply.

If +5V or +12V is not output, the fan motor does not rotate. Connect the DC voltmeter to CN9 and check +5V, +12V and -12V.

Pin No.	Color	Description
1	GRAY	GND
2	GRAY	GND
3	BLACK	GND
4	BLACK	GND
5	RED	+5V
6	RED	+5V
7	YELLOW	-12V
8	ORANGE	+12V

Table 8-2

* Check the CG.

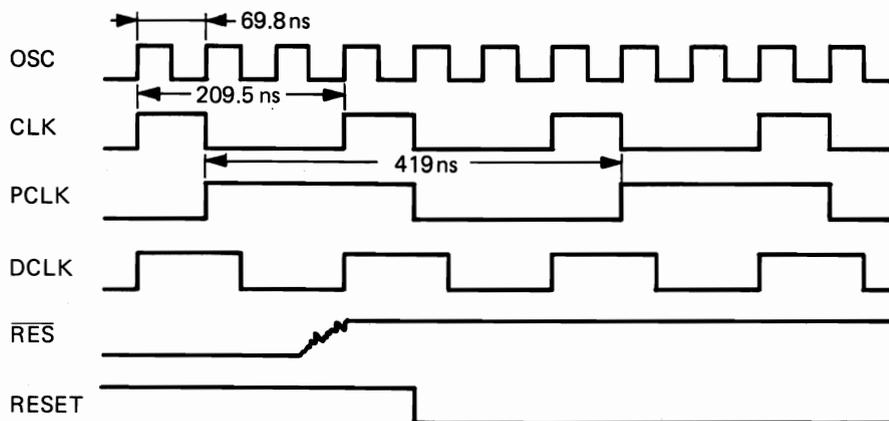


Figure 8-13

* Check the BCU.

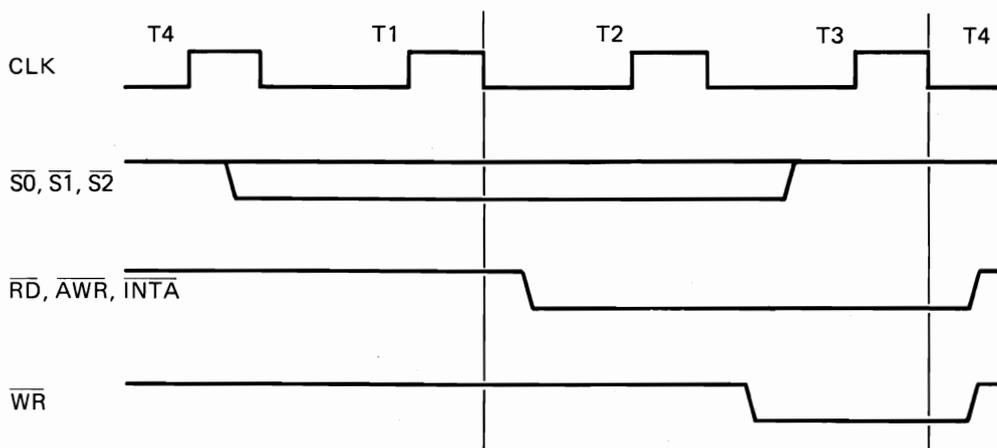


Figure 8-14

* Check the ROM.

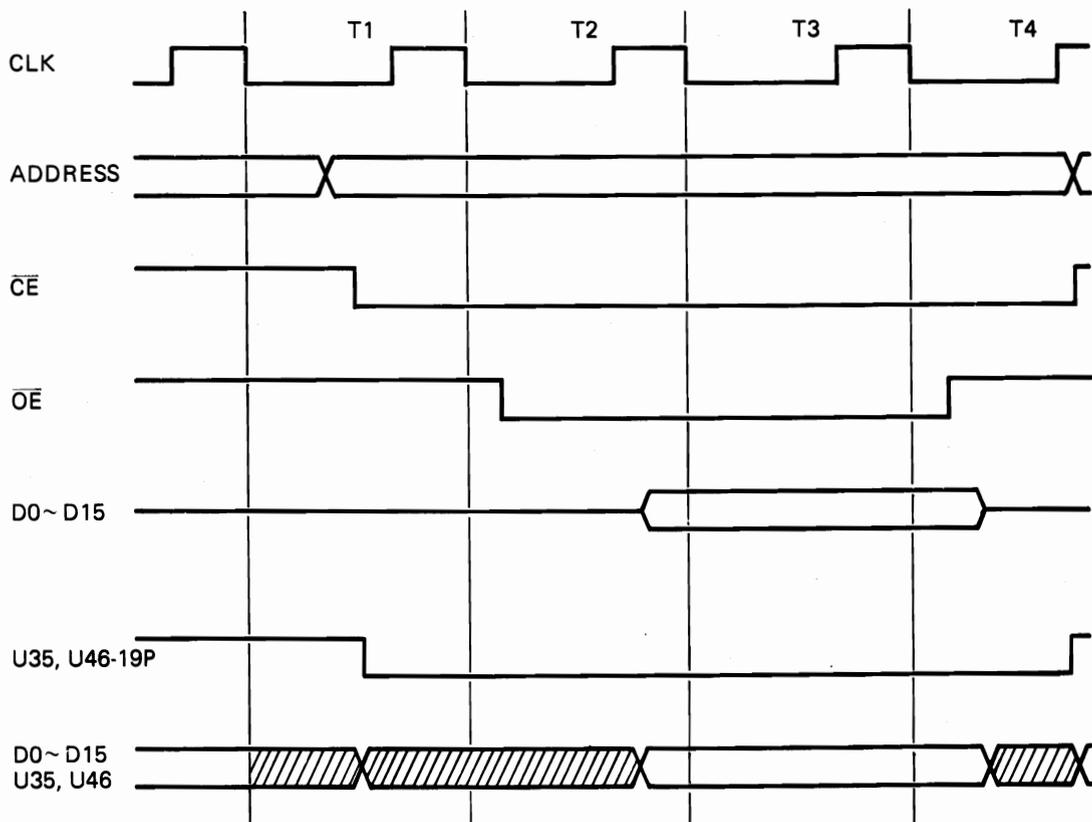


Figure 8-15

* ROM Address Flow

Address	Contents		
FFFF0	EA5B000F0	JMP	F000:E05B
FE05B	FA	CLI	
FE05C	FC	CLD	
FE05D	8CC8	MOV	AX,CS
FE05F	8ED8	MOV	DS,AX
FE061	BE70E0	MOV	SI,E070
FE064	AD	LODSW	
FE065	3DFFFF	CMP	AX,FFFF
FE068	741D	JZ	E087
FE06A	8BD0	MOV	DX,AX
FE06C	AC	LODSB	
FE06D	EE	OUT	DX,AL
FE06E	EBF4	JMP	E064
FE070	B80301		
FE073	D803		
FE075	008300FF		
FE079	63		
FE07A	00996100		

Table 8-3

* Check the PIT.

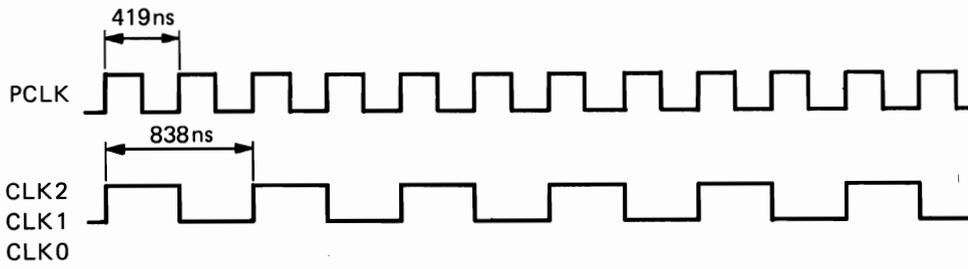


Figure 8-16

* Check the system RAM.

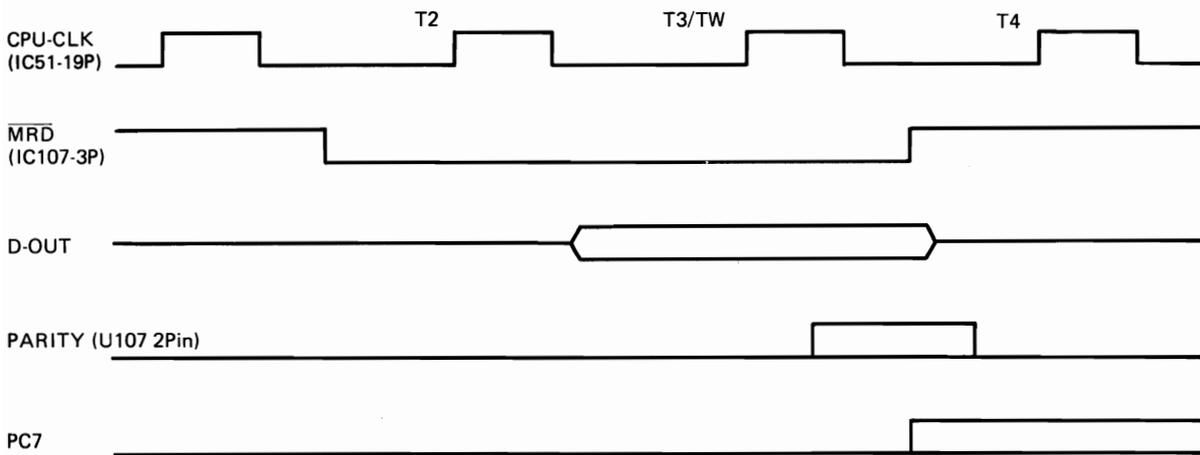


Figure 8-17

* Check the DMAC.

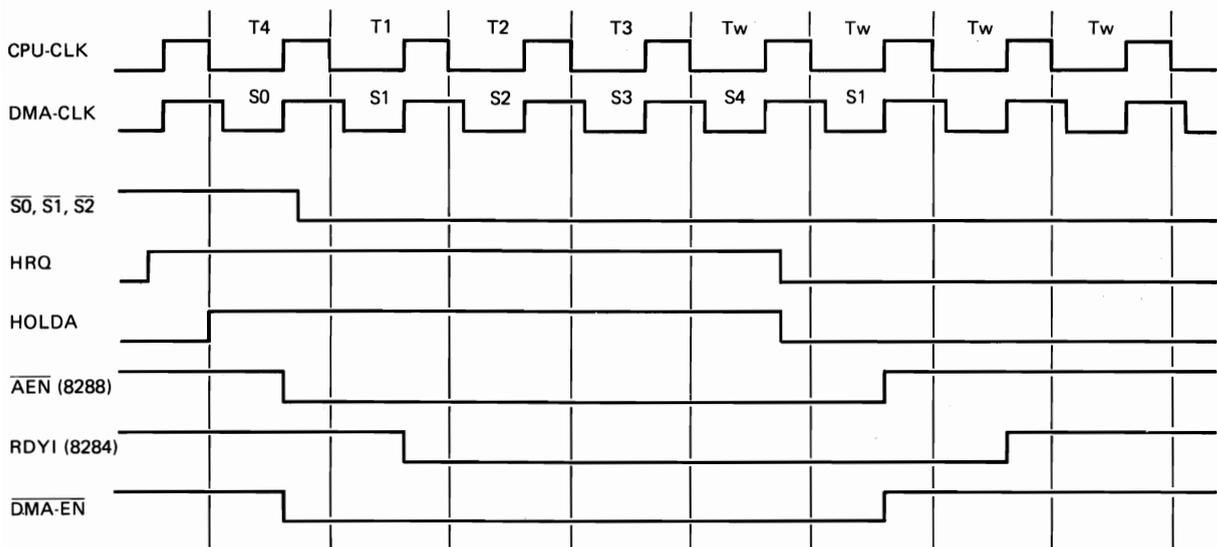


Figure 8-18

PART IX

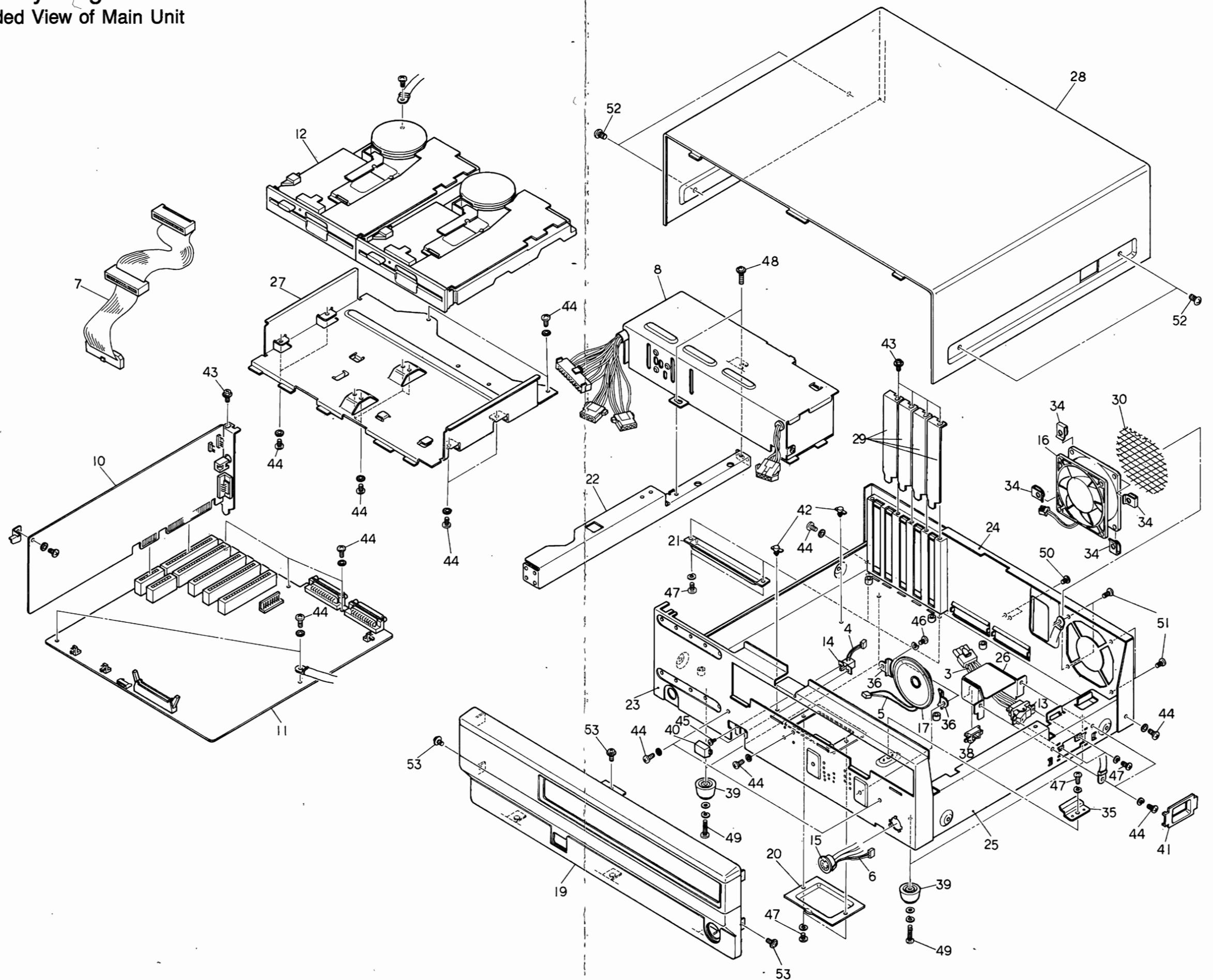
DIAGRAMS AND PARTS LIST

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IX-1. Assembly Diagrams and Parts List

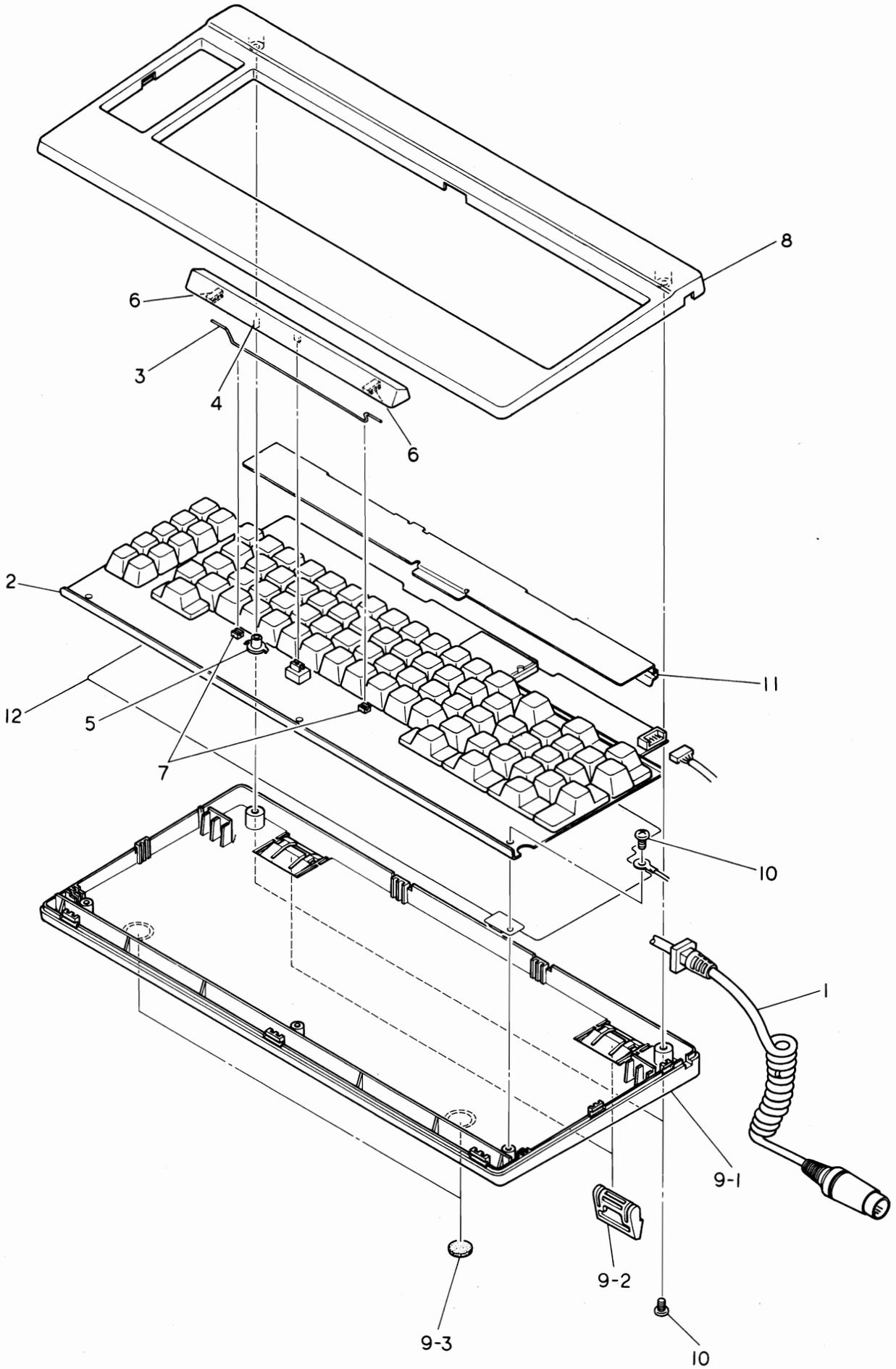
IX-1-1. Exploded View of Main Unit



IX-1-2. Mechanical and Assembly Parts

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
1	SY1-1083-000	1	AC CORD ASSEMBLY	for 240V
1	SY1-1085-000	1	AC CORD ASSEMBLY	for 230V
3	SY1-1087-000	1	CONNECTION CORD ASSEMBLY	POWER UNIT TO POWER SWITCH
4	SY1-0804-000	1	CONNECTION CORD ASSEMBLY	MAIN P.W.B TO RESET SWITCH
5	SY1-0805-000	1	CONNECTION CORD ASSEMBLY	MAIN P.W.B TO SPEAKER
6	SY1-0806-000	1	CONNECTION CORD ASSEMBLY	MAIN P.W.B TO KEYBOARD COM
7	SY1-0807-000	1	CONNECTION CORD ASSEMBLY	MAIN P.W.B. TO FDD
8	SY7-3705-000	1	POWER SUPPLY UNIT	
10		1	MONOCHROME DISPLAY BOARD ASSEMBLY	MODEL M1 AND M2
10		1	COLOR DISPLAY BOARD ASSEMBLY	MODEL C1 AND C2
11		1	MAIN P.W.B. ASSEMBLY	
12		1	FLOPPY DISK DRIVE MDD-211	MODEL M1 AND C1
12		2	FLOPPY DISK DRIVE MDD-211	MODEL M2 AND C2
13	SY1-1086-000	1	POWER SWITCH	
14	SY1-0809-000	1	PUSH SWITCH	RESET
15	SY1-0810-000	1	KEYBOARD CONNECTION JACK	
16	SY1-0811-000	1	FAN MOTOR ASSEMBLY	
17	SY1-0812-000	1	SPEAKER	
19	SY1-0999-000	1	FRONT COVER ASSEMBLY	
20	SY1-0989-000	1	BOTTOM CASE COVER	
21		1	SLOT BRACKET COVER	
22		1	CENTER ARM	
23		1	FRONT PANEL	
24	SY1-1084-000	1	REAR PANEL	
25		1	BOTTOM CASE	
26		1	POWER SWITCH GUARD	
27		1	FDD MOUNTING BRACKET	
28	SY1-0991-000	1	TOP COVER	
29	SY1-0992-000	4	SLOT BRACKET (1)	
30	SY1-0993-000	1	FINGER GUARD	
34	SY1-0994-000	4	FAN BRACKET	
35	SY1-0995-000	1	P.W.B. SUPPORT	
36		2	BRACKET	
38		1	EDGE SADDLE	
39	SY1-1000-000	4	PLASTIC FOOT	
40	SY1-0996-000	1	RESET SWITCH KNOB	
41	SY1-0997-000	1	POWER SWITCH COVER	
42		5	PUSH SPACER	
43	SY1-1100-000	5	HEX HEAD SCREW W/FW M3.5 X 6	
44	XB6-7300-605	23	BIND HEAD SCREW M3 X 6	
45	XB6-7200-405	2	CEMS SCREW M2 X 4	
46	XB1-1300-407	2	CEMS SCREW M3 X 4	
47	XB6-6300-605	7	CEMS SCREW M3 X 6	
48	XB6-7301-205	2	TP SCREW M3 X 12	
49	XB1-1301-605	4	W-CEMS SCREW M3 X 14	
50	XB1-1300-605	2	PAN HEAD SCREW M3 X 6	
51	XB1-1401-007	4	PAN HEAD SCREW M4 X 10	
52	XB1-2400-607	4	TRUSS HEAD SCREW	
53	XB6-7300-605	3	TP SCREW M3 X 6	

IX-1-3. Exploded View of Keyboard



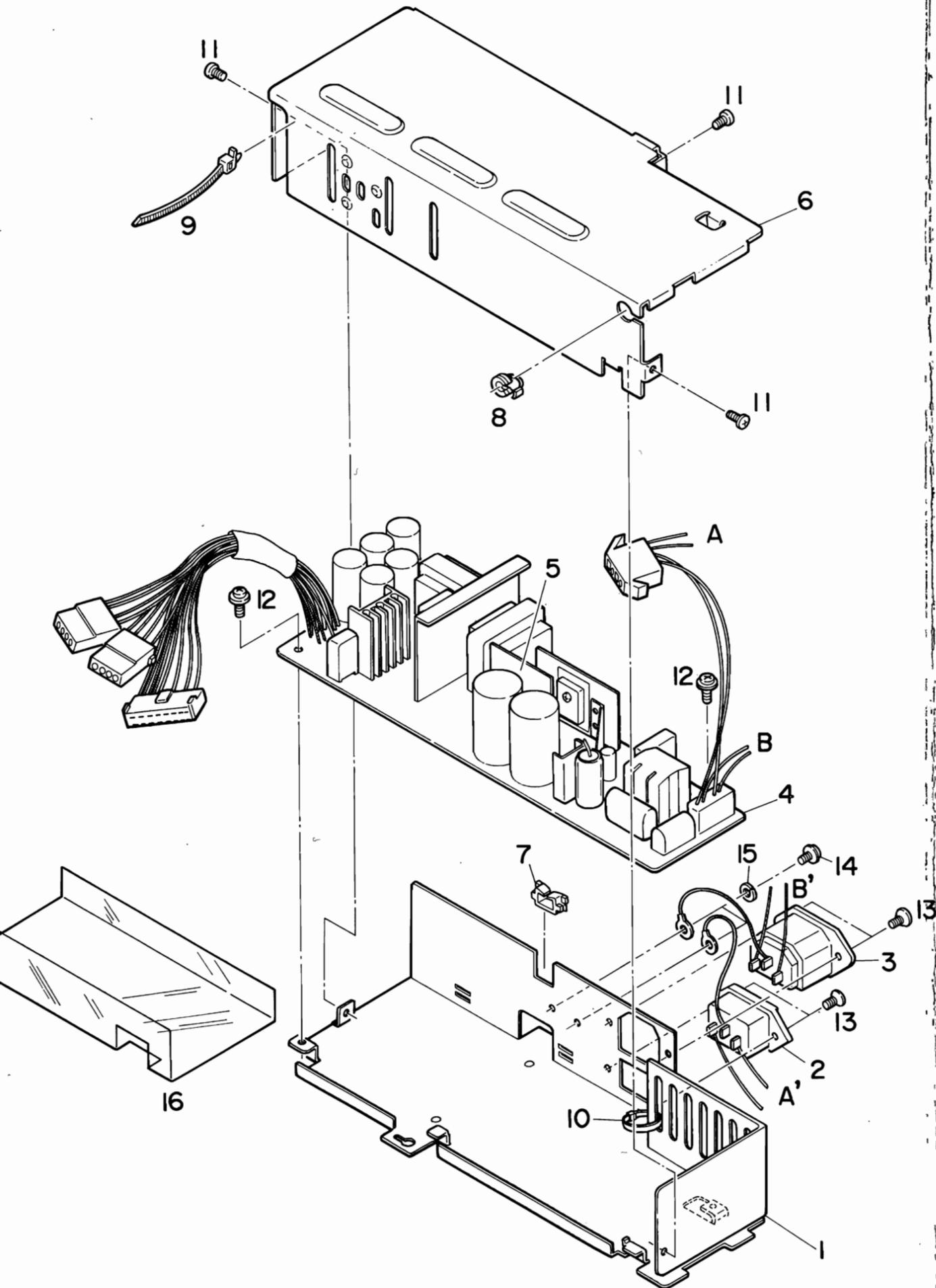
IX-1-4. Keyboard Parts

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
C1	VC1-1161-107	1	ELECTROLYTIC CAPACITOR 100MF 16V	
C2	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C3	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C4	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C5	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C6	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C7	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C8	SY1-0942-000	1	CAPACITOR ARRAY 300PF X 2 50V	
C9	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C10	VC1-1161-106	1	ELECTROLYTIC CAPACITOR 10MF 16V	
C11	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V	
CN1	SY1-0940-000	1	CONNECTOR	
X1	SY1-0941-000	1	CERAMIC OSCILLATOR 6MHz	
D1				
D83	SY1-0943-000	83	DIODE 1S1555	
U1	SY1-0944-000	1	IC MPD8748D OR MPD8048	
U2	WA3-0335-000	1	IC SN74LS125N	
U3	WA3-1012-000	1	IC HD14069B	
U4	WA3-1012-000	1	IC HD14069B	
U5	WA3-1012-000	1	IC HD14069B	
U6	WA3-1012-000	1	IC HD14069B	
R1	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R2	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R3	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R4	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R5	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R6	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R7	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R8	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R9	VR1-1143-512	1	CARBON RESISTOR 5.1K OHM 1/4W 5%	
R10	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R11	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R12	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R13	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R14	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R15	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R16	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R17	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R18	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R19	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R20	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W 5%	
R21	VR1-1143-103	1	CARBON RESISTOR 10K OHM 1/4W 5%	
	SY1-0853-000	1	KEY SWITCH	FOR SPACEBAR
	SY1-0854-000	82	KEY SWITCH	OTHERS
	SY1-0855-000	1	KEY TOP <F3>	ASCII U.K. FRANCE GERMANY
	SY1-0856-000	1	KEY TOP <F4>	* * * *
	SY1-0857-000	1	KEY TOP <F5>	* * * *
	SY1-0858-000	1	KEY TOP <F6>	* * * *
	SY1-0859-000	1	KEY TOP <->	* * * *
	SY1-0860-000	1	KEY TOP <A>	* * * *
	SY1-0861-000	1	KEY TOP <D>	* * * *
	SY1-0862-000	1	KEY TOP <E>	* * * *
	SY1-0863-000	1	KEY TOP <F>	* * * *
	SY1-0864-000	1	KEY TOP <G>	* * * *
	SY1-0865-000	1	KEY TOP <H>	* * * *
	SY1-0866-000	1	KEY TOP <I>	* * * *
	SY1-0867-000	1	KEY TOP <J>	* * * *
	SY1-0868-000	1	KEY TOP <K>	* * * *
	SY1-0869-000	1	KEY TOP <L>	* * * *
	SY1-0870-000	1	KEY TOP <O>	* * * *
	SY1-0871-000	1	KEY TOP <P>	* * * *
	SY1-0872-000	1	KEY TOP <Q>	* * * *
	SY1-0873-000	1	KEY TOP <R>	* * * *
	SY1-0874-000	1	KEY TOP <S>	* * * *
	SY1-0875-000	1	KEY TOP <T>	* * * *
	SY1-0876-000	1	KEY TOP <U>	* * * *

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
	SY1-0877-000	1	KEY TOP <W>	* * *
	SY1-0878-000	1	KEY TOP <Y>	* * *
	SY1-0879-000	1	KEY TOP <; :>	* * *
	SY1-0880-000	1	KEY TOP <' ">	* * *
	SY1-0881-000	1	KEY TOP <^ ~>	* * *
	SY1-0882-000	1	KEY TOP <[>	* * *
	SY1-0883-000	1	KEY TOP <]]>	* * *
	SY1-0884-000	1	KEY TOP <4 ←>	* * * *
	SY1-0885-000	1	KEY TOP <5 →>	* * * *
	SY1-0886-000	1	KEY TOP <6 →>	* * * *
	SY1-0887-000	1	KEY TOP <7 Home>	* * * *
	SY1-0888-000	1	KEY TOP <8 ↑>	* * * *
	SY1-0889-000	1	KEY TOP <9 PgUp>	* * * *
	SY1-2851-000	1	KEY TOP <' @>	* * *
	SY1-2852-000	1	KEY TOP <# ~>	* * *
	SY1-2853-000	1	KEY TOP <Z>	* * *
	SY1-2854-000	1	KEY TOP ACCENT KEY	* * *
	SY1-2855-000	1	KEY TOP <* \$>	* * *
	SY1-2856-000	1	KEY TOP <M>	* * *
	SY1-2857-000	1	KEY TOP <§ ù>	* * *
	SY1-2858-000	1	KEY TOP <£ μ>	* * *
	SY1-2859-000	1	KEY TOP <Z>	* * *
	SY1-2860-000	1	KEY TOP <0>	* * *
	SY1-2861-000	1	KEY TOP <+ *>	* * *
	SY1-2862-000	1	KEY TOP <ö>	* * *
	SY1-2863-000	1	KEY TOP <Ä>	* * *
	SY1-2864-000	1	KEY TOP <# ^>	* * *
	SY1-0890-000	1	KEY TOP TAB	* * * *
	SY1-0891-000	1	KEY TOP <CTRL>	* * * *
	SY1-0892-000	1	KEY TOP ENTER	* * * *
	SY1-0893-000	1	KEY TOP <+>	* * * *
	SY1-0894-000	1	KEY TOP <F1>	* * * *
	SY1-0895-000	1	KEY TOP <F2>	* * * *
	SY1-0896-000	1	KEY TOP <F7>	* * * *
	SY1-0897-000	1	KEY TOP <F8>	* * * *
	SY1-0898-000	1	KEY TOP <F9>	* * * *
	SY1-0899-000	1	KEY TOP <F10>	* * * *
	SY1-0900-000	1	KEY TOP SHIFT-LEFT	* * * *
	SY1-0901-000	1	KEY TOP <1 !>	* * * *
	SY1-0902-000	1	KEY TOP <2 @>	* * * *
	SY1-0903-000	1	KEY TOP <3 #>	* * * *
	SY1-0904-000	1	KEY TOP <4 \$>	* * * *
	SY1-0905-000	1	KEY TOP <5 %>	* * * *
	SY1-0906-000	1	KEY TOP <6 ^>	* * * *
	SY1-0907-000	1	KEY TOP <7 &>	* * * *
	SY1-0908-000	1	KEY TOP <8 *>	* * * *
	SY1-0909-000	1	KEY TOP <9 (>	* * * *
	SY1-0910-000	1	KEY TOP <0)>	* * * *
	SY1-0911-000	1	KEY TOP 	* * * *
	SY1-0912-000	1	KEY TOP <C>	* * * *
	SY1-0913-000	1	KEY TOP <M>	* * * *
	SY1-0914-000	1	KEY TOP <N>	* * * *
	SY1-0915-000	1	KEY TOP <V>	* * * *
	SY1-0916-000	1	KEY TOP <X>	* * * *
	SY1-0917-000	1	KEY TOP <Z>	* * * *
	SY1-0918-000	1	KEY TOP <- ->	* * * *
	SY1-0919-000	1	KEY TOP <= +>	* * * *
	SY1-0920-000	1	KEY TOP <\ >	* * * *
	SY1-0921-000	1	KEY TOP <, <>	* * * *
	SY1-0922-000	1	KEY TOP <. >>	* * * *
	SY1-0923-000	1	KEY TOP </ ?>	* * * *
	SY1-0924-000	1	KEY TOP <1 End>	* * * *
	SY1-0925-000	1	KEY TOP <2 ↓>	* * * *
	SY1-0926-000	1	KEY TOP <3 PgDn>	* * * *
	SY1-2901-000	1	KEY TOP <2 ">	* * * *
	SY1-2902-000	1	KEY TOP <3 £>	* * * *
	SY1-2903-000	1	KEY TOP <1 &>	* * * *
	SY1-2904-000	1	KEY TOP <2 é>	* * * *
	SY1-2905-000	1	KEY TOP <3 ">	* * * *
	SY1-2906-000	1	KEY TOP <4 />	* * * *
	SY1-2907-000	1	KEY TOP <5 (>	* * * *
	SY1-2908-000	1	KEY TOP <6 \$>	* * * *
	SY1-2909-000	1	KEY TOP <7 è>	* * * *
	SY1-2910-000	1	KEY TOP <8 !>	* * * *
	SY1-2911-000	1	KEY TOP <9 ç>	* * * *
	SY1-2912-000	1	KEY TOP <0 à>	* * * *
	SY1-2913-000	1	KEY TOP <°)>	* * * *

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
	SY1-2914-000	1	KEY TOP <> .<>	* *
	SY1-2915-000	1	KEY TOP <W>	*
	SY1-2916-000	1	KEY TOP <? ,>	*
	SY1-2917-000	1	KEY TOP <. ;>	*
	SY1-2918-000	1	KEY TOP </ :>	*
	SY1-2919-000	1	KEY TOP <+ =>	*
	SY1-2920-000	1	KEY TOP <3 §>	*
	SY1-2921-000	1	KEY TOP <6 &>	*
	SY1-2922-000	1	KEY TOP <7 />	*
	SY1-2923-000	1	KEY TOP <8 (>	*
	SY1-2924-000	1	KEY TOP <0 =>	*
	SY1-2925-000	1	KEY TOP <β ?>	*
	SY1-2926-000	1	KEY TOP <^ \>	*
	SY1-2927-000	1	KEY TOP <Y>	*
	SY1-2928-000	1	KEY TOP <, ;>	*
	SY1-2929-000	1	KEY TOP <. :>	*
	SY1-2930-000	1	KEY TOP <9)>	*
	SY1-0927-000	1	KEY TOP LEFT ARROW	* * * *
	SY1-0928-000	1	KEY TOP <NUM LOCK>	* * * *
	SY1-0929-000	1	KEY TOP <SCROLL LOCK>	* * * *
	SY1-0930-000	1	KEY TOP SHIFT-RIGHT	* * * *
	SY1-0931-000	1	KEY TOP <CAPS LOCK>	* * * *
	SY1-0932-000	1	KEY TOP <ALT>	* * * *
	SY1-0933-000	1	KEY TOP <INS>	* * * *
	SY1-0934-000	1	KEY TOP 	* * * *
	SY1-0935-000	1	KEY TOP SPACEBAR	* * * *
	SY1-0947-000	1	KEY TOP <ESC>	* * * *
	SY1-0948-000	1	KEY TOP <PRT SC>	* * * *
1	SY1-0802-000	1	CURL CORD ASSEMBLY	
2	SY1-0851-000	1	PANEL	
3	SY1-0852-000	1	LEVER	
4	SY1-0936-000	1	GUIDE PIN	FOR SPACEBAR
5	SY1-0937-000	1	GUIDE	FOR SPACEBAR
6	SY1-0938-000	2	LEVER GUIDE A	FOR SPACEBAR
7	SY1-0939-000	2	LEVER GUIDE B	FOR SPACEBAR
8	SY1-0945-000	1	KEYBOARD TOP CASE	
9	SY1-0946-000	1	KEYBOARD BOTTOM ASSEMBLY	
9-2	SY1-0949-000	2	KEYBOARD TILT STAND	
9-3	SY1-0950-000	2	RUBBER FOOT	
10	XB3-1300-807	3	PAN HEAD P TITE SCREW M3 X 8	
11		1	KEYBOARD COVER	
12		1	SHIELD PLATE	

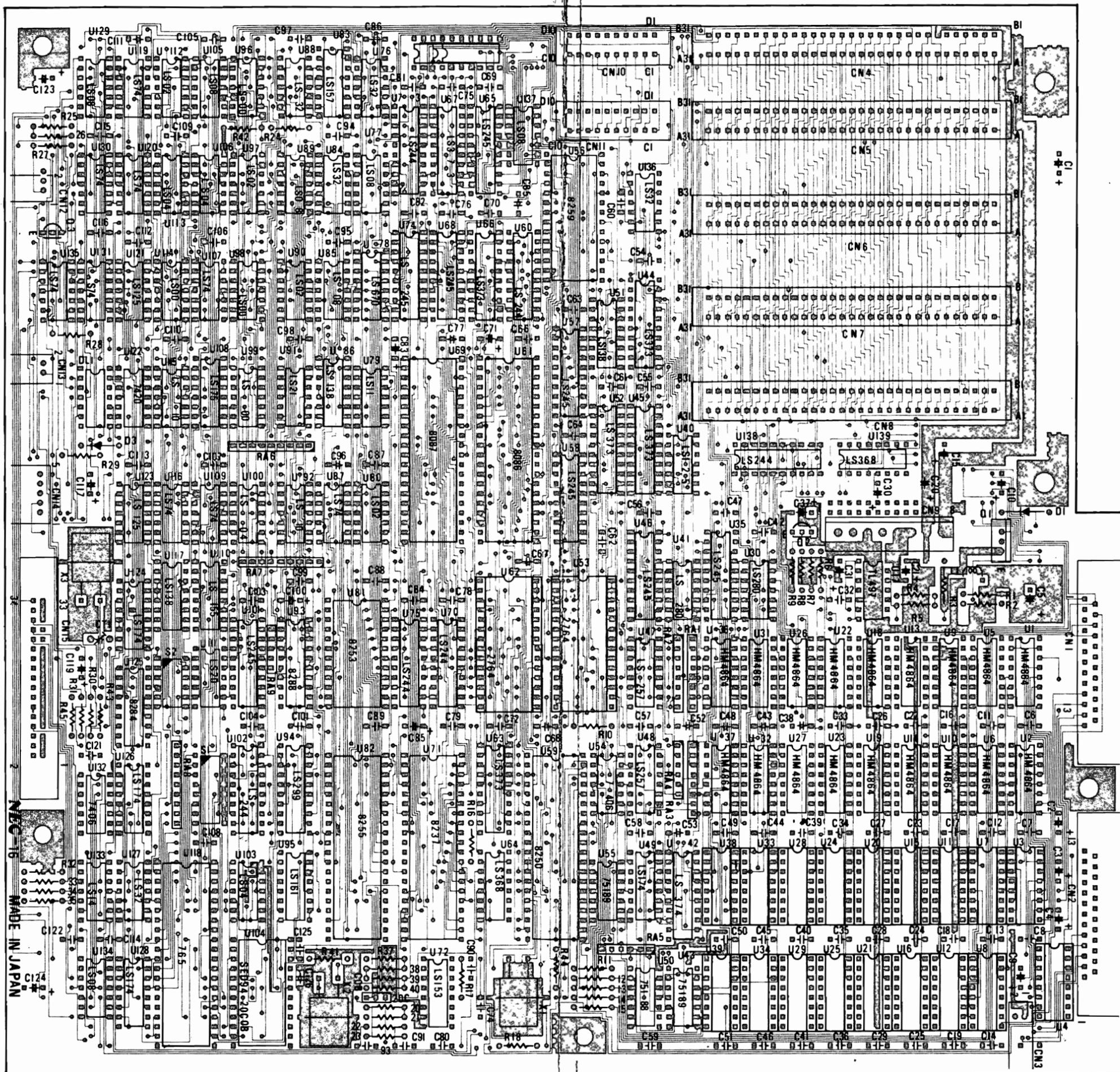
IX-1-5. Exploded View of Power Supply Unit



IX-1-6. Power Supply Unit Parts

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
1		1	BOTTOM CASE	
2	SY1-1080-000	1	INLET ASSEMBLY	
3	SY1-1081-000	1	OUTLET ASSEMBLY	
4		1	P.W.BOARD ASSEMBLY	
5		1	P.W.BOARD ASSEMBLY	
6		1	TOP CASE	
7	SY1-0814-000	1	EDGE SADDLE	
8	SY1-1082-000	1	CORD BUSH	
9		1	SNAP BAND	
10		1	INSULATION TIE	
11	XB6-6300-605	3	CEMS SCREW M3 X 6	
12	XB6-7300-605	2	TP SCREW M3 X 6	
13	XB1-3300-605	4	FLAT HEAD SCREW M3 X 6	
14	XB6-7400-605	2	TP SCREW M4 X 6	
15		2	SPRING WASHER M4.5 X 7	
16		1	INSULATION SHEET	

IX-1-7. Main P.C.B. Assembly Diagram



IX-1.8. Main P.C.B. Parts

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
Q3	X65-6360-000	1	TRANSISTOR 2SC945	NO-RANK
D3	SY1-0848-000	1	SILICON DIODE MA150	
S1	WC8-0050-000	1	DIP SWITCH KTD-08	
S2	WC8-0014-000	1	DIP SWITCH KTD-06	
DL1	SY1-0960-000	1	DELAY LINE DCE 10-35	
X1	SY1-0959-000	1	CRYSTAL 1.8432MHZ	
X2	WK2-0057-000	1	CRYSTAL 16.0MHZ	
X3	SY1-0065-000	1	CRYSTAL 14.31818MHZ	
CN1	WS2-0035-000	1	CONNECTOR DB-25SA-N50L3	
CN2	SY1-0984-000	1	CONNECTOR DB-25PA-N50L3	
CN3	SY1-0964-000	1	CONNECTOR 5046-02A	
CN4	SY1-0977-000	1	CONNECTOR H421021-31	
CN5	SY1-0977-000	1	CONNECTOR H421021-31	
CN6	SY1-0977-000	1	CONNECTOR H421021-31	
CN7	SY1-0977-000	1	CONNECTOR H421021-31	
CN8	SY1-0977-000	1	CONNECTOR H421021-31	
CN9	SY1-0966-000	1	CONNECTOR B8P-VH	
CN10	SY1-0979-000	1	CONNECTOR H421021-10	
CN11	SY1-0979-000	1	CONNECTOR H421021-10	
CN12	SY1-0964-000	1	CONNECTOR 5046-02A	
CN13	SY1-0964-000	1	CONNECTOR 5046-02A	
CN14	SY1-0965-000	1	CONNECTOR S5B-XH-A	
CN15	VS1-0143-034	1	CONNECTOR 3431-2002	
	WA9-0059-000	1	IC SOCKET DICF-40CS	
	WA9-0058-000	2	IC SOCKET DICF-28CS	
RA1	SY1-0987-000	1	RESISTOR ARRAY 33 OHM X 4	
RA2	SY1-0987-000	1	RESISTOR ARRAY 33 OHM X 4	
RA3	SY1-0987-000	1	RESISTOR ARRAY 33 OHM X 4	
RA4	SY1-0982-000	1	RESISTOR ARRAY 1K OHM X 5	
RA6	SY1-0986-000	1	RESISTOR ARRAY 4.7K OHM X 8	
RA7	SY1-0983-000	1	RESISTOR ARRAY 1K OHM X 8	
RA8	SY1-0986-000	1	RESISTOR ARRAY 4.7K OHM X 8	
RA9	SY1-0985-000	1	RESISTOR ARRAY 4.7K OHM X 4	
R10	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R11	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R12	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R13	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R14	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R15	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R16	VR1-1143-472	1	CARBON RESISTOR 4.7K OHM 1/4W 5%	
R17	VR1-1143-105	1	CARBON RESISTOR 1M OHM 1/4W 5%	
R18	VR1-1143-202	1	CARBON RESISTOR 2K OHM 1/4W 5%	
R20	VR1-1143-101	1	CARBON RESISTOR 100 OHM 1/4W 5%	
R22	VR1-1143-221	1	CARBON RESISTOR 220 OHM 1/4W 5%	
R24	VR1-1143-472	1	CARBON RESISTOR 4.7K OHM 1/4W 5%	
R25	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R26	VR1-1143-301	1	CARBON RESISTOR 300 OHM 1/4W 5%	
R27	VR1-1143-330	1	CARBON RESISTOR 33 OHM 1/4W 5%	
R28	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R29	VR1-1143-103	1	CARBON RESISTOR 10K OHM 1/4W 5%	
R30	VR1-1143-472	1	CARBON RESISTOR 4.7K OHM 1/4W 5%	
R31	VR1-1143-472	1	CARBON RESISTOR 4.7K OHM 1/4W 5%	
R32	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R33	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R34	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R35	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R37	VR1-1143-010	1	CARBON RESISTOR 1 OHM 1/4W 5%	
R38	VR1-1143-561	1	CARBON RESISTOR 560 OHM 1/4W 5%	
R39	VR1-1143-221	1	CARBON RESISTOR 220 OHM 1/4W 5%	
R40	VR1-1143-561	1	CARBON RESISTOR 560 OHM 1/4W 5%	

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
R41	VR1-1143-754	1	CARBON RESISTOR 750K OHM 1/4W 5%	
R42	VR1-1143-472	1	CARBON RESISTOR 4.7K OHM 1/4W 5%	
R43	VR1-1143-330	1	CARBON RESISTOR 33 OHM 1/4W 5%	
R44	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R45	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
R46	VR1-1143-330	1	CARBON RESISTOR 33 OHM 1/4W 5%	
	XB3-1260-807	2	PAN HEAD TAPPING SCREW M2.6 X 8	
	XB6-6300-805	4	CEMS SCREW M3 X 8 SW	
U1	WA3-1557-000	1	IC MB8264A-15	
U2	WA3-1557-000	1	IC MB8264A-15	
U3	WA3-1557-000	1	IC MB8264A-15	
U4	WA3-1557-000	1	IC MB8264A-15	
U5	WA3-1557-000	1	IC MB8264A-15	
U6	WA3-1557-000	1	IC MB8264A-15	
U7	WA3-1557-000	1	IC MB8264A-15	
U8	WA3-1557-000	1	IC MB8264A-15	
U9	WA3-1557-000	1	IC MB8264A-15	
U10	WA3-1557-000	1	IC MB8264A-15	
U11	WA3-1557-000	1	IC MB8264A-15	
U12	WA3-1557-000	1	IC MB8264A-15	
U13	WA3-1557-000	1	IC MB8264A-15	
U14	WA3-1557-000	1	IC MB8264A-15	
U15	WA3-1557-000	1	IC MB8264A-15	
U16	WA3-1557-000	1	IC MB8264A-15	
U18	WA3-1557-000	1	IC MB8264A-15	
U19	WA3-1557-000	1	IC MB8264A-15	
U20	WA3-1557-000	1	IC MB8264A-15	
U21	WA3-1557-000	1	IC MB8264A-15	
U22	WA3-1557-000	1	IC MB8264A-15	
U23	WA3-1557-000	1	IC MB8264A-15	
U24	WA3-1557-000	1	IC MB8264A-15	
U25	WA3-1557-000	1	IC MB8264A-15	
U26	WA3-1557-000	1	IC MB8264A-15	
U27	WA3-1557-000	1	IC MB8264A-15	
U28	WA3-1557-000	1	IC MB8264A-15	
U29	WA3-1557-000	1	IC MB8264A-15	
U30	WA3-0316-000	1	IC SN74LS280N	
U31	WA3-1557-000	1	IC MB8264A-15	
U32	WA3-1557-000	1	IC MB8264A-15	
U33	WA3-1557-000	1	IC MB8264A-15	
U34	WA3-1557-000	1	IC MB8264A-15	
U35	WA3-0361-000	1	IC SN74LS245N	
U36	WA3-1557-000	1	IC MB8264A-15	
U37	WA3-1557-000	1	IC MB8264A-15	
U38	WA3-1557-000	1	IC MB8264A-15	
U39	WA3-1557-000	1	IC MB8264A-15	
U40	WA3-0335-000	1	IC SN74LS125AN	
U41	WA3-0316-000	1	IC SN74LS280N	
U42	WA3-0281-000	1	IC SN74LS374N	
U43	WA3-0320-000	1	IC SN75189AN	
U44	WA3-0428-000	1	IC SN74LS373N	
U45	WA3-0428-000	1	IC SN74LS373N	
U46	WA3-0361-000	1	IC SN74LS245N	
U47	WA3-0427-000	1	IC SN74LS257N	
U48	WA3-0427-000	1	IC SN74LS257N	
U49	WA3-0142-000	1	IC SN74LS174N	
U50	WA3-0319-000	1	IC SN75188N	
U51	WA3-0110-000	1	IC SN74LS138N	
U52	WA3-0428-000	1	IC SN74LS373N	
U53	EY3-0173-000	1	IC HN482764G-3	
U54	X65-7160-000	1	IC SN7406N	
U55	WA3-0320-000	1	IC SN75189AN	
U56	WA3-0805-000	1	IC MPD8259AC	
U57	WA3-0361-000	1	IC SN74LS245N	
U58	WA3-0361-000	1	IC SN74LS245N	
U59	SY1-0849-000	1	IC WD8250PL-00	
U60	WA3-0336-000	1	IC SN74LS244N	
U61	SY1-0835-000	1	IC MPD8086D	
U62	EY3-0172-000	1	IC HN482764G-3	
J63	WA3-0428-000	1	IC SN74LS373N	
U64	WA3-0145-000	1	IC SN74LS368AN	

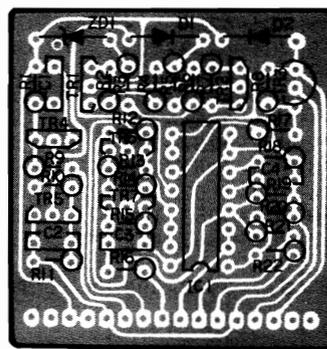
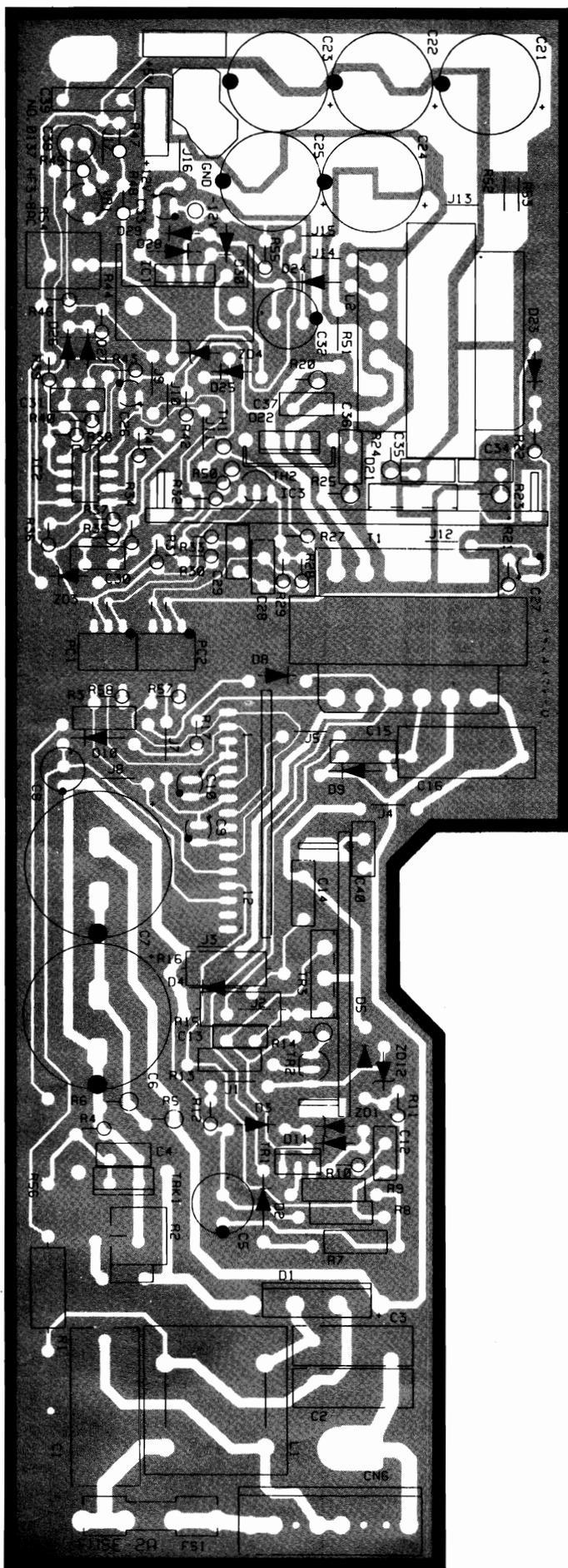
KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
U65	WA3-0361-000	1	IC SN74LS245N	
U66	WA3-0428-000	1	IC SN74LS373N	
U67	WA3-0428-000	1	IC SN74LS373N	
U68	WA3-0361-000	1	IC SN74LS245N	
U70	WA3-0336-000	1	IC SN74LS244N	
U71	SY1-0847-000	1	IC MPD8237AC-5	
U72	WA3-0283-000	1	IC SN74LS153N	
U73	WA3-0336-000	1	IC SN74LS244N	
U74	WA3-0361-000	1	IC SN74LS245N	
U75	WA3-0336-000	1	IC SN74LS244N	
U76	WA3-0135-000	1	IC SN74LS32N	
U77	WA3-0134-000	1	IC SN74LS08N	
U78	WA3-0371-000	1	IC SN74LS670N	
U79	X65-7527-000	1	IC SN74LS11N	
U80	WA3-0148-000	1	IC SN74LS02N	
U81	WA3-0810-000	1	IC MPD8253C-5	
U82	WA3-0944-000	1	IC MPD8255AC-5	
U83	X65-7468-000	1	IC SN74LS157N	
U84	WA3-0135-000	1	IC SN74LS32N	
U85	WA3-0134-000	1	IC SN74LS08N	
U86	WA3-0110-000	1	IC SN74LS138N	
U87	WA3-0137-000	1	IC SN74LS74AN	
U88	WA3-0135-000	1	IC SN74LS32N	
U89	WA3-0134-000	1	IC SN74LS08N	
U90	WA3-0148-000	1	IC SN74LS02N	
U91	X65-7528-000	1	IC SN74LS21N	
U92	WA3-0143-000	1	IC SN74LS10N	
U93	WA3-0806-000	1	IC MPB8288D	
U94	WA3-0365-000	1	IC SN74LS299N	
U95	WA3-0275-000	1	IC SN74LS161AN	
U96	WA3-0132-000	1	IC SN74LS00N	
U97	WA3-0148-000	1	IC SN74LS02N	
U98	WA3-0132-000	1	IC SN74LS00N	
U99	WA3-0132-000	1	IC SN74LS00N	
U100	X65-7467-000	1	IC SN74LS04N	
U101	WA3-0361-000	1	IC SN74LS245N	
U102	WA3-0336-000	1	IC SN74LS244N	
U103	WA3-0820-000	1	IC HD74LS04P	
U104	WA3-1155-000	1	IC SED9420COB	
U105	WA3-0134-000	1	IC SN74LS08N	
U106	X65-7467-000	1	IC SN74LS04N	
U107	WA3-0137-000	1	IC SN74LS74AN	
U108	WA3-0138-000	1	IC SN74LS175N	
U109	WA3-0137-000	1	IC SN74LS74AN	
U110	WA3-0181-000	1	IC SN74LS155N	
U111	WA3-0170-000	1	IC SN74LS20N	
U112	WA3-0148-000	1	IC SN74LS02N	
U113	X65-7467-000	1	IC SN74LS04N	
U114	WA3-0132-000	1	IC SN74LS00N	
U115	WA3-0143-000	1	IC SN74LS10N	
U116	WA3-0137-000	1	IC SN74LS74AN	
U117	WA3-0110-000	1	IC SN74LS138N	
U118	WA3-0529-000	1	IC MPD765AC	
U119	WA3-0137-000	1	IC SN74LS74AN	
U120	WA3-0137-000	1	IC SN74LS74AN	
U121	WA3-0335-000	1	IC SN74LS125AN	
U122	X65-7144-000	1	IC SN7420N	
U123	WA3-0335-000	1	IC SN74LS125AN	
U124	WA3-0142-000	1	IC SN74LS174N	
U125	WA3-1038-000	1	IC MPB8284AD	
U126	WA3-0142-000	1	IC SN74LS174N	
U127	WA3-0135-000	1	IC SN74LS32N	
U128	WA3-0142-000	1	IC SN74LS174N	
U129	WA3-0134-000	1	IC SN74LS08N	
U130	WA3-0137-000	1	IC SN74LS74AN	
U131	WA3-0289-000	1	IC SN74S74N	
U132	X65-7160-000	1	IC SN7406N	
U133	WA3-0002-000	1	IC SN74LS14N	
U134	WA3-0134-000	1	IC SN74LS08N	
U135	WA3-0137-000	1	IC SN74LS74AN	
U136	WA3-0135-000	1	IC SN74LS32N	
U137	WA3-0134-000	1	IC SN74LS08N	
U138	WA3-0336-000	1	IC SN74LS244N	
U139	WA3-0145-000	1	IC SN74LS368AN	
U140	WA3-0135-000	1	IC SN74LS32N	

use HITACHI's IC only

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
C1	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C2	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C3	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C4	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C6	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C7	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C8	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25v	
C9	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C11	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C12	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C13	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C14	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C15	VC2-3252-226	1	TANTALUM CAPACITOR 22MF 25V 20%	
C16	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C17	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C18	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C19	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C20	VC2-3252-226	1	TANTALUM CAPACITOR 22MF 25V 20%	
C22	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C23	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C24	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C25	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C26	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C27	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C28	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C29	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C30	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C33	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C34	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C35	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C36	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C38	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C39	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C40	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C41	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C42	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C43	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C44	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C45	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C46	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C47	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C48	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C49	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C50	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C51	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C52	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C53	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C54	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C55	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C56	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C57	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C58	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C59	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C60	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C61	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C62	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C63	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C64	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C65	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C66	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C67	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C68	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C69	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C70	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C71	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C72	VC4-4254-104	1	CANTALUM CAPACITOR 0.1MF 25V	
C74	VC4-1501-100	1	CERAMIC CAPACITOR 10PF 50V SL	
C75	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C76	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C77	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C78	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C79	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C80	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C81	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C82	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
C83	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C84	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C85	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C86	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C87	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C88	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C89	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C90	SY1-0963-000	1	CERAMIC CAPACITOR 51PF 10%	
C91	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C94	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C95	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C96	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C97	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C98	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C99	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C100	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C101	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C103	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C104	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C105	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C106	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C107	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C108	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C109	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C110	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C111	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C112	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C113	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C114	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C115	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C116	VC4-3253-103	1	CERAMIC CAPACITOR 0.01MF 25V 10%	
C117	VC1-1161-476	1	ELECTROLYTIC CAPACITOR 47MF 16V	
C119	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C121	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C122	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C123	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C124	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C125	VC4-3253-103	1	CERAMIC CAPACITOR 0.01MF 25V 10%	
C127	VC4-3503-472	1	CERAMIM CAPACITOR 4700PF 50V 10%	
CT1	SY1-0970-000	1	TRIMMER CAPACITOR MAX20P	

IX-1-9. Power Supply P.C.B. Assembly Diagram



IX-1-10. Power Supply P.C.B. Parts

• Main P.C.B.

Marked with "*" ...Applicable serial Nos. are 231251 ~ and 431251 ~.

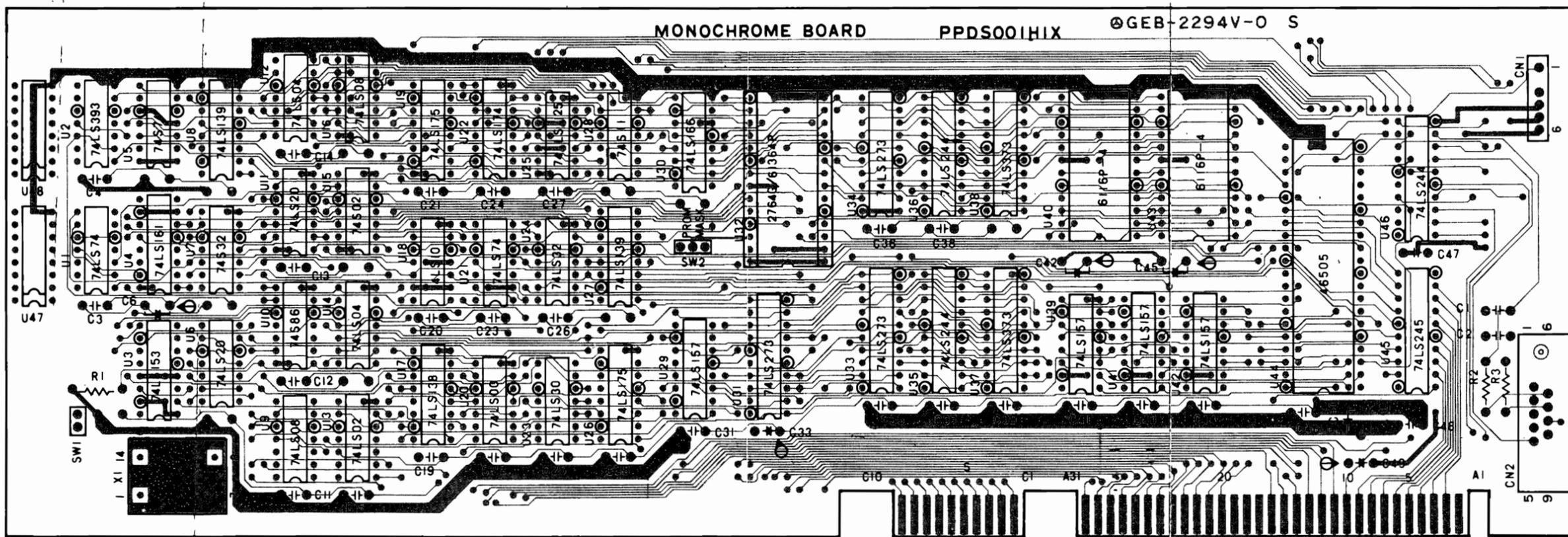
KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
TR1	SY1-1037-000	1	TRANSISTOR 2SA1357	Y RANK
TR2	WA2-0237-000	1	TRANSISTOR 2SC2655	Y RANK
TR3	SY1-1038-000	1	TRANSISTOR 2SC3262	
IC1	WA4-0216-000	1	IC HA178M12	
IC2	SY1-1039-000	1	IC uPC358C	
IC3	SY1-1040-000	1	IC TL431CLP-B	
F1	SY1-1047-000	1	FUSE 250V 2A	
TH1	SY1-1048-000	1	THERMAL LEAD FUSE 95°C	
D1	SY1-1031-000	1	SILICON DIODE KBL06LM	
D2	SY1-1032-000	1	SILICON DIODE V19C	
D3	X65-5435-000	1	SILICON DIODE 1S2076A	
D4	SY1-1030-000	1	SILICON DIODE PLR818	
D5	SY1-1030-000	1	SILICON DIODE PLR818	
D6	SY1-1033-000	1	SILICON DIODE 1SS81	
D7	SY1-1033-000	1	SILICON DIODE 1SS81	
D8	SY1-1033-000	1	SILICON DIODE 1SS81	
D9	SY1-1030-000	1	SILICON DIODE PLR818	
D10	SY1-1032-000	1	SILICON DIODE V19C	
D11	X65-5435-000	1	SILICON DIODE 1S2076A	
D21	SY1-1035-000	1	SILICON DIODE C25P049	
D22	SY1-1034-000	1	SILICON DIODE C10P06Q	
D23	SY1-1033-000	1	SILICON DIODE 1SS81	
D24	SY1-1029-000	1	SILICON DIODE EGP10D	
D25	X65-5435-000	1	SILICON DIODE 1S2076A	
D26	X65-5435-000	1	SILICON DIODE 1S2076A	
D27	X65-5435-000	1	SILICON DIODE 1S2076A	
D28	SY1-1032-000	1	SILICON DIODE V19C	
D29	SY1-1033-000	1	SILICON DIODE 1SS81	
ZD1	WA1-0095-000	1	ZENER DIODE HZ3A1	*
ZD1	WA1-0110-000	1	ZENER DIODE HZ6A1	
ZD3	WA1-0110-000	1	ZENER DIODE HZ6A1	
ZD4	WA1-0212-000	1	ZENER DIODE HZ12C3	
ZD12	WA1-0095-000	1	ZENER DIODE HZ3A1	
TRK1	SY1-1042-000	1	THYRISTOR SM12G41	
L1	SY1-1050-000	1	CHOKO COIL	
L2	SY1-1049-000	1	CHOKO COIL	
T1	SY1-1043-000	1	POWER TRANSFORMER	
FH1	SY1-1045-000	2	FUSE HOLDER	
B1		3	CEMS SCREW M3 X 6	
B2		3	CEMS SCREW M3 X 10	
R1	SY1-1073-000	1	METAL-OXIDE RESISTOR 33K OHM 2W	
R2	SY1-1079-000	1	CEMENT RESISTOR ASSY	
R3	SY1-1074-000	1	METAL-OXIDE RESISTOR 47 OHM 2W	
R4	VR1-1143-101	1	CARBON RESISTOR 100 OHM 1/4W	
R5	VR1-1123-224	1	CARBON RESISTOR 220K OHM 1/2W	
R6	VR1-1123-224	1	CARBON RESISTOR 220K OHM 1/2W	
R7	SY1-1067-000	1	METAL-OXIDE RESISTOR 0.33 OHM 1W	
R8	SY1-1071-000	1	METAL-OXIDE RESISTOR 220 OHM 1W	
R9	SY1-1068-000	1	METAL-OXIDE RESISTOR 1 OHM 1W	
R10	VR1-1143-101	1	CARBON RESISTOR 100 OHM 1/4W	
R11	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W	
R12	VR1-1143-332	1	CARBON RESISTOR 3.3K OHM 1/4W	
R13	SY1-1070-000	1	METAL-OXIDE RESISTOR 15 OHM 1W	
R14	VR1-1143-339	1	CARBON RESISTOR 3.3 OHM 1/4W	
R15	SY1-1069-000	1	METAL-OXIDE RESISTOR 0.22 OHM 2W	
R16	SY1-1072-000	1	METAL-OXIDE RESISTOR 100 OHM 2W	
R17	VR1-1143-010	1	CARBON RESISTOR 1 OHM 1/4W	
R18	VR1-1143-101	1	CARBON RESISTOR 100 OHM 1/4W	

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
R20	VR1-1123-220	1	CARBON RESISTOR 22 OHM 1/2W	
R21	VR1-1143-101	1	CARBON RESISTOR 100 OHM 1/4W	
R22	VR1-1143-100	1	CARBON RESISTOR 10 OHM 1/4W	
R23	VR1-1123-220	1	CARBON RESISTOR 22 OHM 1/2W	
R24	VR1-1123-220	1	CARBON RESISTOR 22 OHM 1/2W	
R25	VR1-1123-220	1	CARBON RESISTOR 22 OHM 1/2W	
R27	VR1-1143-103	1	CARBON RESISTOR 10K OHM 1/4W	
R28	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W	*
R28	VR1-1143-103	1	CARBON RESISTOR 10K OHM 1/4W	
R29	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W	
R30	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W	
R31	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W	
R32	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W	
R33	VR1-1143-103	1	CARBON RESISTOR 10K OHM 1/4W	
R34	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W	
R35	VR1-1143-153	1	CARBON RESISTOR 15K OHM 1/4W	
R36	VR1-1143-912	1	CARBON RESISTOR 9.1K OHM 1/4W	*
R36	VR1-1143-103	1	CARBON RESISTOR 10K OHM 1/4W	
R37	VR1-1143-822	1	CARBON RESISTOR 8.2K OHM 1/4W	*
R37	VR1-1143-103	1	CARBON RESISTOR 10K OHM 1/4W	
R38	VR1-1143-153	1	CARBON RESISTOR 15K OHM 1/4W	
R39	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W	*
R39	VR1-1143-391	1	CARBON RESISTOR 390 OHM 1/4W	
R40	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W	
R41	VR1-1143-151	1	CARBON RESISTOR 150 OHM 1/4W	
R42	VR1-1143-151	1	CARBON RESISTOR 150 OHM 1/4W	
R43	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W	*
R43	VR1-1143-391	1	CARBON RESISTOR 390 OHM 1/4W	
R44	VR1-1143-152	1	CARBON RESISTOR 1.5K OHM 1/4W	
R45	VR1-1143-272	1	CARBON RESISTOR 2.7K OHM 1/4W	
R46	VR1-1143-104	1	CARBON RESISTOR 100K OHM 1/4W	
R47	VR1-1143-682	1	CARBON RESISTOR 6.8K OHM 1/4W	
R48	VR1-1143-223	1	CARBON RESISTOR 22K OHM 1/4W	
R50	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W	
R51	SY1-1076-000	1	MANGANESE WIRE	
R52	SY1-1076-000	1	MANGANESE WIRE	
R53	SY1-1076-000	1	MANGANESE WIRE	
R54	SY1-1078-000	1	CEMENT RESISTOR 47 OHM 5W	
R55	SY1-1077-000	1	FUSE RESISTOR 10 OHM 1/4W	
R56	VR1-1143-684	1	CARBON RESISTOR 680K OHM 1/4W	
R57	VR1-1143-684	1	CARBON RESISTOR 680K OHM 1/4W	
VR1	SY1-1075-000	1	SEMI-FIXED RESISTOR 1K OHM	
C1	SY1-1057-000	1	FILM CAPACITOR 0.47MF 250V	*
C1	SY1-1028-000	1	FILM CAPACITOR 0.1MF 250V	
C2	SY1-1054-000	1	CERAMIC CAPACITOR 2200PF 250V	
C3	SY1-1054-000	1	CERAMIC CAPACITOR 2200PF 250V	
C4	VC3-2501-103	1	FILM CAPACITOR 0.01MF 50V	
C5	SY1-1060-000	1	ELECTROLYTIC CAPACITOR 470MF 16V	
C6	SY1-1066-000	1	ELECTROLYTIC CAPACITOR 270MF 250V	
C7	SY1-1066-000	1	ELECTROLYTIC CAPACITOR 270MF 250V	
C8	SY1-1065-000	1	ELECTROLYTIC CAPACITOR 47MF 50V	
C9	SY1-1063-000	1	ELECTROLYTIC CAPACITOR 10MF 50V	
C10	SY1-1063-000	1	ELECTROLYTIC CAPACITOR 10MF 50V	
C11	SY1-1063-000	1	ELECTROLYTIC CAPACITOR 10MF 50V	
C12	SY1-1056-000	1	FILM CAPACITOR 0.1MF 50V	
C13	SY1-1056-000	1	FILM CAPACITOR 0.1MF 50V	
C14	SY1-1053-000	1	CERAMIC CAPACITOR 1000PF 2000V	
C15	SY1-1052-000	1	CERAMIC CAPACITOR 100PF 2000V	
C16	SY1-1055-000	1	FILM CAPACITOR 0.047MF 630V	
C21	SY1-1059-000	1	ELECTROLYTIC CAPACITOR 6800MF 10V	
C22	SY1-1059-000	1	ELECTROLYTIC CAPACITOR 6800MF 10V	
C23	SY1-1059-000	1	ELECTROLYTIC CAPACITOR 6800MF 10V	
C24	SY1-1059-000	1	ELECTROLYTIC CAPACITOR 6800MF 10V	
C25	SY1-1061-000	1	ELECTROLYTIC CAPACITOR 3300MF 25V	
C26	SY1-1063-000	1	ELECTROLYTIC CAPACITOR 10MF 50V	
C27	SY1-1063-000	1	ELECTROLYTIC CAPACITOR 10MF 50V	
C28	SY1-1056-000	1	FILM CAPACITOR 0.1MF 50V	
C29	VC3-2501-103	1	FILM CAPACITOR 0.01MF 50V	
C30	SY1-1056-000	1	FILM CAPACITOR 0.1MF 50V	
C31	SY1-1056-000	1	FILM CAPACITOR 0.1MF 50V	
C32	SY1-1062-000	1	ELECTROLYTIC CAPACITOR 220MF 35V	
C33	SY1-1063-000	1	ELECTROLYTIC CAPACITOR 10MF 50V	
C34	VC3-2501-103	1	FILM CAPACITOR 0.01MF 50V	
C35	VC3-2501-103	1	FILM CAPACITOR 0.01MF 50V	

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
C36	VC3-2501-103	1	FILM CAPACITOR 0.01MF 50V	
C37	VC3-2501-103	1	FILM CAPACITOR 0.01MF 50V	
C38	SY1-1064-000	1	ELECTROLYTIC CAPACITOR 4.7MF 50V	
C39	SY1-1058-000	1	FILM CAPACITOR 0.01MF 630V	
C40	VC3-2501-103	1	FILM CAPACITOR 0.01MF 50V	
HS1		1	HEAT SINK	
HS2		1	HEAT SINK	
HS3		1	HEAT SINK	
HS4		1	HEAT SINK	
PC1	SY1-1041-000	1	PHOTO COUPLER	*
PC1	SY1-1096-000	1	PHOTO COUPLER	
PC2	SY1-1041-000	1	PHOTO COUPLER	*
PC2	SY1-1096-000	1	PHOTO COUPLER	
CN1	SY1-1046-000	1	CONNECTOR	

• Sub P.C.B.

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
TR1	SY1-1036-000	1	TRANSISTOR 2SA1048	Y RANK
TR2	WA2-0197-000	1	TRANSISTOR 2SC2458	Y RANK
TR3	WA2-0236-000	1	TRANSISTOR 2SA1020	Y RANK
TR4	SY1-1036-000	1	TRANSISTOR 2SA1048	Y RANK
TR5	WA2-0197-000	1	TRANSISTOR 2SC2458	Y RANK
TR6	SY1-1036-000	1	TRANSISTOR 2SA1048	Y RANK
TR7	WA2-0197-000	1	TRANSISTOR 2SC2458	Y RANK
IC1	SY1-0836-000	1	IC uPD494C	
R1	VR1-1143-472	1	CARBON RESISTOR 4.7K OHM 1/4W 5%	
R2	VR1-1143-332	1	CARBON RESISTOR 3.3K OHM 1/4W 5%	
R3	VR1-1143-332	1	CARBON RESISTOR 3.3K OHM 1/4W 5%	
R4	VR1-1143-472	1	CARBON RESISTOR 4.7K OHM 1/4W 5%	
R5	VR1-1143-332	1	CARBON RESISTOR 3.3K OHM 1/4W 5%	
R6	VR1-1143-103	1	CARBON RESISTOR 10K OHM 1/4W 5%	
R7	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R8	VR1-1143-101	1	CARBON RESISTOR 100 OHM 1/4W 5%	
R9	VR1-1143-153	1	CARBON RESISTOR 15K OHM 1/4W 5%	
R10	VR1-1143-153	1	CARBON RESISTOR 15K OHM 1/4W 5%	
R11	VR1-1143-472	1	CARBON RESISTOR 4.7K OHM 1/4W 5%	
R12	VR1-1143-223	1	CARBON RESISTOR 22K OHM 1/4W 5%	
R13	VR1-1143-152	1	CARBON RESISTOR 1.5K OHM 1/4W 5%	
R14	VR1-1143-152	1	CARBON RESISTOR 1.5K OHM 1/4W 5%	
R15	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R16	VR1-1143-101	1	CARBON RESISTOR 100 OHM 1/4W 5%	
R17	VR1-1143-151	1	CARBON RESISTOR 150 OHM 1/4W 5%	
R18	VR1-1143-223	1	CARBON RESISTOR 22K OHM 1/4W 5%	
R19	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R20	VR1-1143-103	1	CARBON RESISTOR 10K OHM 1/4W 5%	
R21	VR1-1143-101	1	CARBON RESISTOR 100 OHM 1/4W 5%	
R22	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
C1	VC3-2501-103	1	MYLAR CAPACITOR 0.01MF 50V	
C2	VC3-2501-103	1	MYLAR CAPACITOR 0.01MF 50V	
C3	VC3-2501-103	1	MYLAR CAPACITOR 0.01MF 50V	
C4	VC3-2501-102	1	MYLAR CAPACITOR 0.001MF 50V	
D1	X65-5435-000	1	SILICON DIODE 1S2076A	
D2	X65-5435-000	1	SILICON DIODE 1S2076A	
ZD1	WA1-0110-000	1	ZENER DIODE HZ6A1	
CN1	SY1-1051-000	1	CONNECTOR	

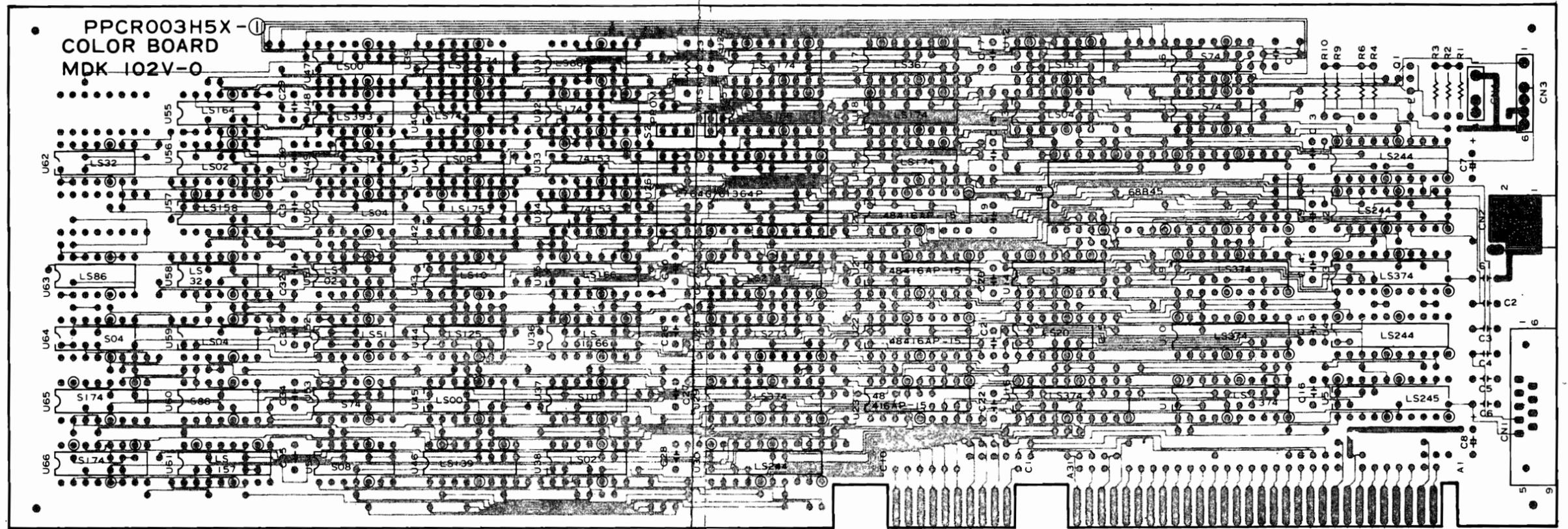


IX-1-12. Monochrome Display Adapter Board Parts

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
CN2	SY1-1090-000	1	CONNECTOR, OUTPUT 9 PIN	
	WA9-0058-000	1	IC SOCKET	
X1	SY1-1099-000	1	CRYSTAL MODULE 16.257MHz	
R1	VR1-1143-472	1	CARBON RESISTOR 4.7K OHM 1/4W 5%	
R2	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R3	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
	SY1-0998-000	1	SLOT SUPPORTER	
	XB6-7300-605	1	BIND HEAD SCREW	
	XB6-6300-805	2	CEMS SCREW	
U1	WA3-0137-000	1	IC SN74LS74AN	
U2	WA3-0282-000	1	IC SN74LS393N	
U3	WA3-0283-000	1	IC SN74LS153N	
U4	WA3-0275-000	1	IC SN74LS161AN	
U5	WA3-0289-000	1	IC SN74LS74N	
U6	WA3-0170-000	1	IC SN74LS20N	
U7	WA3-0378-000	1	IC SN74S32N	
U8	WA3-0200-000	1	IC SN74LS139N	
U9	WA3-0134-000	1	IC SN74LS08N	
U10	WA3-0290-000	1	IC SN74S86N	
U11	WA3-0170-000	1	IC SN74LS20N	
U12	X65-7467-000	1	IC SN74LS04N	
U13	WA3-0148-000	1	IC SN74LS02N	
U14	X65-7467-000	1	IC SN74LS04N	
U15	WA3-0373-000	1	IC SN74S02N	
U16	WA3-0134-000	1	IC SN74LS08N	
U17	WA3-0110-000	1	IC SN74LS138N	
U18	WA3-0143-000	1	IC SN74LS10N	
U19	WA3-0138-000	1	IC SN74LS175N	
U20	WA3-0132-000	1	IC SN74LS00N	
U21	WA3-0137-000	1	IC SN74LS74AN	
U22	WA3-0142-000	1	IC SN74LS174N	
U23	WA3-0213-000	1	IC SN74LS30N	
U24	WA3-0135-000	1	IC SN74LS32N	
U25	WA3-0335-000	1	IC SN74LS125AN	
U26	WA3-0138-000	1	IC SN74LS175N	
U27	WA3-0200-000	1	IC SN74LS139N	
U28	WA3-0376-000	1	IC SN74S11N	
U29	X65-7468-000	1	IC SN74LS157N	
U30	WA3-0212-000	1	IC SN74LS166AN	
U31	WA3-0279-000	1	IC SN74LS273N	
U32	SY1-1095-000	1	IC ROM CHARACTER GENERATOR	
U33	WA3-0279-000	1	IC SN74LS273N	
U34	WA3-0279-000	1	IC SN74LS273N	
U35	WA3-0336-000	1	IC SN74LS244N	
U36	WA3-0336-000	1	IC SN74LS244N	
U37	WA3-0428-000	1	IC SN74LS373N	
U38	WA3-0428-000	1	IC SN74LS373N	
U39	X65-7468-000	1	IC SN74LS157N	
U40	WA3-0945-000	1	IC HM6116P-4	
U41	X65-7468-000	1	IC SN74LS157N	
U42	X65-7468-000	1	IC SN74LS157N	
U43	WA3-0945-000	1	IC HM6116P-4	
U44	SY1-0837-000	1	IC HD68B45SP	
U45	WA3-0361-000	1	IC SN74LS245N	
U46	WA3-0336-000	1	IC SN74LS244N	
C1	VC4-2502-220	1	CERAMIC CAPACITOR 22PF 50V 10%	
C2	VC4-2502-220	1	CERAMIC CAPACITOR 22PF 50V 10%	
C3	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C4	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C6	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C11	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C12	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C13	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C14	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C15	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C19	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C20	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C21	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
C22	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C23	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C24	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C25	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C26	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C27	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C28	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C31	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C33	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C35	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C36	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C37	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C38	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C39	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C41	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C42	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C43	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C44	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C45	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C46	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C47	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C48	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C50	VC2-3162-226	1	TANTALUM CAPACITOR 22MF 16V 20%	
C51	VC4-3503-561	1	CERAMIC CAPACITOR 560PF 10%	
C52	VC4-2502-181	1	CERAMIC CAPACITOR 180PF 10%	

IX-1-13. Color Display Adapter Board Assembly Diagram



IX-1-14. Color Display Adapter Board Parts

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
Q1	X65-6360-000	1	TRANSISTOR 2SC945	NO-RANK
CN1	SY1-1090-000	1	CONNECTOR, OUTPUT 9 PIN	
CN2	SY1-1091-000	1	CONNECTOR 2 PIN	
CN3	SY1-1092-000	1	CONNECTOR 5 PIN	
CN4	SY1-1093-000	1	CONNECTOR 3 PIN	
	WA9-0058-000	1	IC SOCKET	
L1	SY1-1094-000	1	CHOKO COIL	
L2	SY1-1094-000	1	CHOKO COIL	
L3	SY1-1094-000	1	CHOKO COIL	
L4	SY1-1094-000	1	CHOKO COIL	
R1	VR1-1143-510	1	CARBON RESISTOR 51 OHM 1/4W 5%	
R2	VR1-1143-101	1	CARBON RESISTOR 100 OHM 1/4W 5%	
R3	VR1-1143-330	1	CARBON RESISTOR 33 OHM 1/4W 5%	
R4	VR1-1143-133	1	CARBON RESISTOR 13K OHM 1/4W 5%	
R6	VR1-1143-332	1	CARBON RESISTOR 3.3K OHM 1/4W 5%	
R9	VR1-1143-222	1	CARBON RESISTOR 2.2K OHM 1/4W 5%	
R10	VR1-1143-562	1	CARBON RESISTOR 5.6K OHM 1/4W 5%	
R11	VR1-1143-562	1	CARBON RESISTOR 5.6K OHM 1/4W 5%	
	SY1-0998-000	1	SLOT SUPPORT	
	XB6-7300-605	1	BIND HEAD SCREW	
	XB6-6300-805	2	CEMS SCREW	
U1	WA3-0336-000	1	IC SN74LS244N	
U2	WA3-0336-000	1	IC SN74LS244N	
U3	WA3-0281-000	1	IC SN74LS374N	
U4	WA3-0336-000	1	IC SN74LS244N	
U5	WA3-0361-000	1	IC SN74LS245N	
U6	WA3-0289-000	1	IC SN74S74N	
U7	WA3-0289-000	1	IC SN74S74N	
U8	SY1-0837-000	1	IC HD68B45SP	
U9	WA3-0281-000	1	IC SN74LS374N	
U10	WA3-0281-000	1	IC SN74LS374N	
U11	WA3-0281-000	1	IC SN74LS374N	
U12	WA3-0356-000	1	IC SN74LS151N	
U13	X65-7467-000	1	IC SN74LS04N	
U14	WA3-0110-000	1	IC SN74LS138N	
U15	WA3-0170-000	1	IC SN74LS20N	
U16	WA3-0281-000	1	IC SN74LS374N	
U17	WA3-0198-000	1	IC SN74LS367AN	
U18	WA3-0142-000	1	IC SN74LS174N	
U19	WA3-0142-000	1	IC SN74LS174N	
U20	SY1-0838-000	1	IC HM48416AP-15	
U21	SY1-0838-000	1	IC HM48416AP-15	
U22	SY1-0838-000	1	IC HM48416AP-15	
U23	SY1-0838-000	1	IC HM48416AP-15	
U24	WA3-0142-000	1	IC SN74LS174N	
U25	WA3-0212-000	1	IC SN74LS166AN	
U26	SY1-1095-000	1	IC ROM CHARACTER GENERATOR	
U27	WA3-0279-000	1	IC SN74LS273N	
U28	SY1-0831-000	1	IC SN74ALS273N	
U29	WA3-0281-000	1	IC SN74LS374N	
U30	WA3-0336-000	1	IC SN74LS244N	
U31	WA3-0139-000	1	IC SN74LS86N	
U32	WA3-0386-000	1	IC SN74S174N	
U33	X65-7455-000	1	IC SN74153N	
U34	X65-7455-000	1	IC SN74153N	
U35	WA3-0212-000	1	IC SN74LS166AN	
U36	WA3-0212-000	1	IC SN74LS166AN	
U37	WA3-0284-000	1	IC SN74S10N	
U38	WA3-0148-000	1	IC SN74LS02N	
U39	WA3-0137-000	1	IC SN74LS74AN	
U40	WA3-0137-000	1	IC SN74LS74AN	
U41	WA3-0375-000	1	IC SN74S08N	
U42	WA3-0138-000	1	IC SN74LS175N	
U43	WA3-0143-000	1	IC SN74LS10N	
U44	WA3-0335-000	1	IC SN74LS125AN	
U45	WA3-0132-000	1	IC SN74LS00N	
U46	WA3-0200-000	1	IC SN74LS139N	

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
U47	WA3-0132-000	1	IC SN74LS00N	
U48	WA3-0282-000	1	IC SN74LS393N	
U49	WA3-0378-000	1	IC SN74S32N	
U50	X65-7467-000	1	IC SN74LS04N	
U51	WA3-0148-000	1	IC SN74LS02N	
U52	WA3-0180-000	1	IC SN74LS51N	
U53	WA3-0289-000	1	IC SN74S74N	
U54	WA3-0375-000	1	IC SN74S08N	
U55	WA3-0229-000	1	IC SN74LS164N	
U56	WA3-0148-000	1	IC SN74LS02N	
U57	WA3-0385-000	1	IC SN74S158N	
U58	WA3-0135-000	1	IC SN74LS32N	
U59	X65-7467-000	1	IC SN74LS04N	
U60	WA3-0290-000	1	IC SN74S86N	
U61	X65-7468-000	1	IC SN74LS157N	
U62	WA3-0135-000	1	IC SN74LS32N	
U63	WA3-0139-000	1	IC SN74LS86N	
U64	WA3-0214-000	1	IC SN74S04N	
U65	WA3-0386-000	1	IC SN74S174N	
U66	WA3-0386-000	1	IC SN74S174N	
C1	VC4-2502-471	1	CERAMIC CAPACITOR 470PF 50V 10%	
C2	VC4-2502-471	1	CERAMIC CAPACITOR 470PF 50V 10%	
C3	VC4-2502-471	1	CERAMIC CAPACITOR 470PF 50V 10%	
C4	VC4-2502-471	1	CERAMIC CAPACITOR 470PF 50V 10%	
C5	VC4-2502-471	1	CERAMIC CAPACITOR 470PF 50V 10%	
C6	VC4-2502-471	1	CERAMIC CAPACITOR 470PF 50V 10%	
C7	VC2-3252-226	1	TANTALUM CAPACITOR 22MF 25V 20%	
C8	VC2-3162-226	1	TANTALUM CAPACITOR 22MF 16V 20%	
C9	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C10	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C11	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C13	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C14	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C15	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C16	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C17	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C18	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C19	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C20	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C21	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C22	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C23	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C26	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C27	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C28	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C29	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C30	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C31	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C32	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C33	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C34	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C35	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	

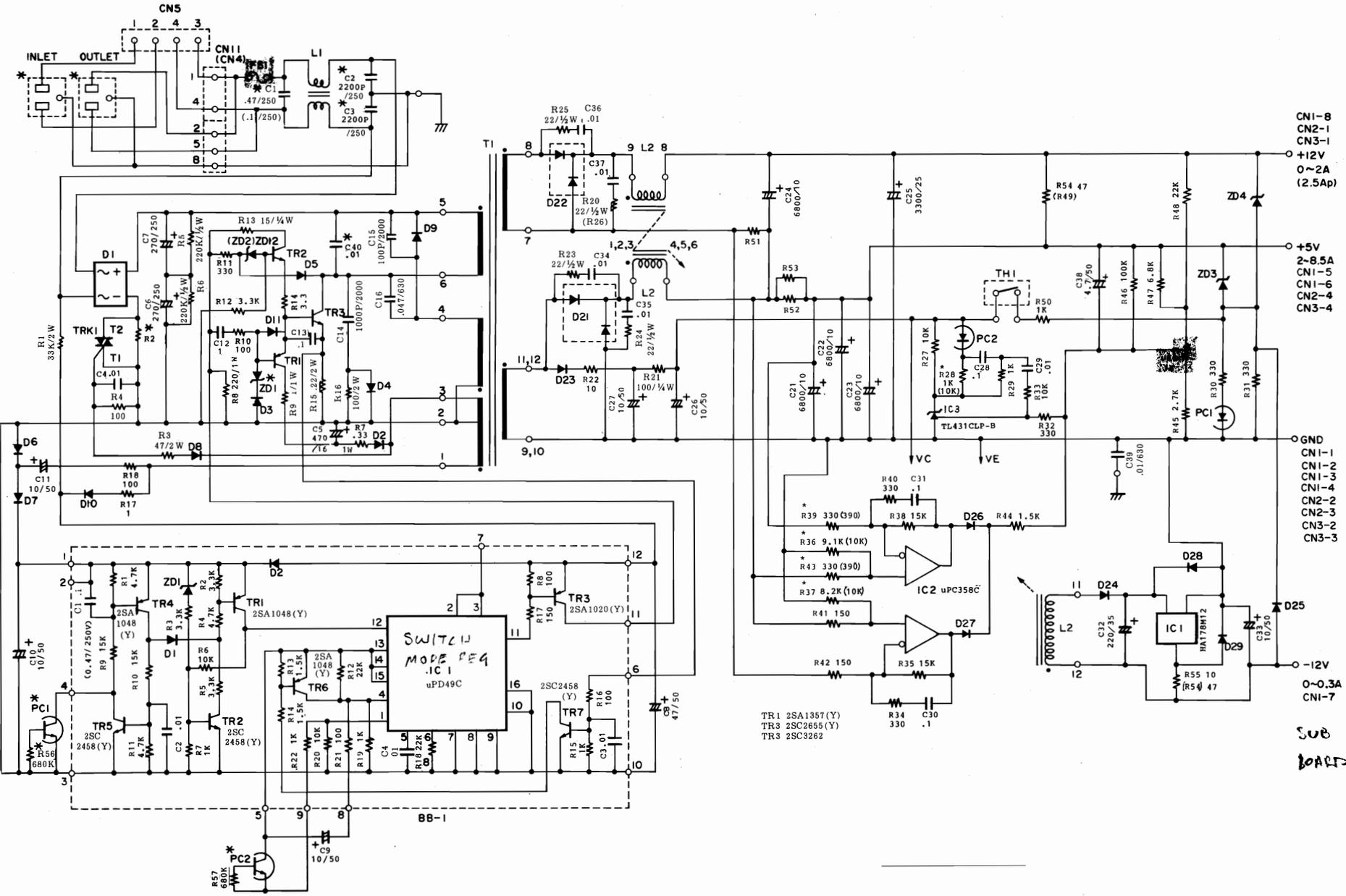
IX-1-16. RAM Board Parts

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
S1	WC8-0014-000	1	DIP SWITCH KTD-06	
R1	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R2	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R3	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R4	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R5	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R6	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R7	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R8	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R9	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R10	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R11	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R12	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R13	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R14	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R15	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R16	VR1-1143-300	1	CARBON RESISTOR 30 OHM 1/4W 5%	
R17	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R18	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R19	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R20	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R21	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R22	VR1-1143-102	1	CARBON RESISTOR 1K OHM 1/4W 5%	
R23	VR1-1143-331	1	CARBON RESISTOR 330 OHM 1/4W 5%	
U1	WA3-0316-000	1	IC SN74LS280N	
U2	WA3-1557-000	1	IC MB8264A-15	
U3	WA3-1557-000	1	IC MB8264A-15	
U4	WA3-1557-000	1	IC MB8264A-15	
U5	WA3-1557-000	1	IC MB8264A-15	
U6	WA3-1557-000	1	IC MB8264A-15	
U7	WA3-1557-000	1	IC MB8264A-15	
U8	WA3-1557-000	1	IC MB8264A-15	
U9	WA3-1557-000	1	IC MB8264A-15	
U10	WA3-1557-000	1	IC MB8264A-15	
U11	WA3-1557-000	1	IC MB8264A-15	
U12	WA3-1557-000	1	IC MB8264A-15	
U13	WA3-1557-000	1	IC MB8264A-15	
U14	WA3-1557-000	1	IC MB8264A-15	
U15	WA3-1557-000	1	IC MB8264A-15	
U16	WA3-1557-000	1	IC MB8264A-15	
U17	WA3-1557-000	1	IC MB8264A-15	
U18	WA3-1557-000	1	IC MB8264A-15	
U19	WA3-1557-000	1	IC MB8264A-15	
U20	WA3-0361-000	1	IC SN74LS245N	
U21	WA3-1557-000	1	IC MB8264A-15	
U22	WA3-1557-000	1	IC MB8264A-15	
U23	WA3-1557-000	1	IC MB8264A-15	
U24	WA3-1557-000	1	IC MB8264A-15	
U25	WA3-1557-000	1	IC MB8264A-15	
U26	WA3-1557-000	1	IC MB8264A-15	
U27	WA3-1557-000	1	IC MB8264A-15	
U28	WA3-1557-000	1	IC MB8264A-15	
U29	WA3-1557-000	1	IC MB8264A-15	
U30	WA3-1557-000	1	IC MB8264A-15	
U31	WA3-1557-000	1	IC MB8264A-15	
U32	WA3-1557-000	1	IC MB8264A-15	
U33	WA3-1557-000	1	IC MB8264A-15	
U34	WA3-1557-000	1	IC MB8264A-15	
U35	WA3-1557-000	1	IC MB8264A-15	
U36	WA3-1557-000	1	IC MB8264A-15	
U37	WA3-1557-000	1	IC MB8264A-15	
U38	WA3-1557-000	1	IC MB8264A-15	
U39	WA3-0316-000	1	IC SN74LS280N	
U40	X65-7144-000	1	IC SN7420N	
U41	WA3-0148-000	1	IC SN74LS02N	
U42	WA3-0134-000	1	IC SN74LS08N	
U43	WA3-0148-000	1	IC SN74LS02N	
U44	SY1-0960-000	1	DELAY LINE DCE 10-35	
U45	WA3-0143-000	1	IC SN74LS10N	
U46	WA3-0148-000	1	IC SN74LS02N	
U47	WA3-0148-000	1	IC SN74LS02N	
U48	WA3-0137-000	1	IC SN74LS74AN	
U49	X65-7467-000	1	IC SN74LS04N	

KEY NO.	PART NO.	Q'TY	DESCRIPTION	REMARK
U50	WA3-0335-000	1	IC SN74LS125AN	
U51	WA3-0427-000	1	IC SN74LS257N	
U52	WA3-0427-000	1	IC SN74LS257N	
U53	WA3-0110-000	1	IC SN74LS138N	
U54	WA3-0134-000	1	IC SN74LS08N	
U55	WA3-0361-000	1	IC SN74LS245N	
C1	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C2	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C3	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C4	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C5	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C6	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C7	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C8	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C9	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C10	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C11	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C12	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C13	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C15	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C16	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C17	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C18	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C19	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C20	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C21	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C22	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C23	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C24	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C25	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C26	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C27	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C28	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C29	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C30	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C31	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C32	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C33	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C34	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C35	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C37	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C38	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C39	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C40	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C41	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C42	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	
C44	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C46	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C47	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C48	VC4-4254-104	1	CERAMIC CAPACITOR 0.1MF 25V	
C49	VC2-3162-106	1	TANTALUM CAPACITOR 10MF 16V 20%	

IX-2-4. Power Supply Unit FOR EXPLANATION SEE P114

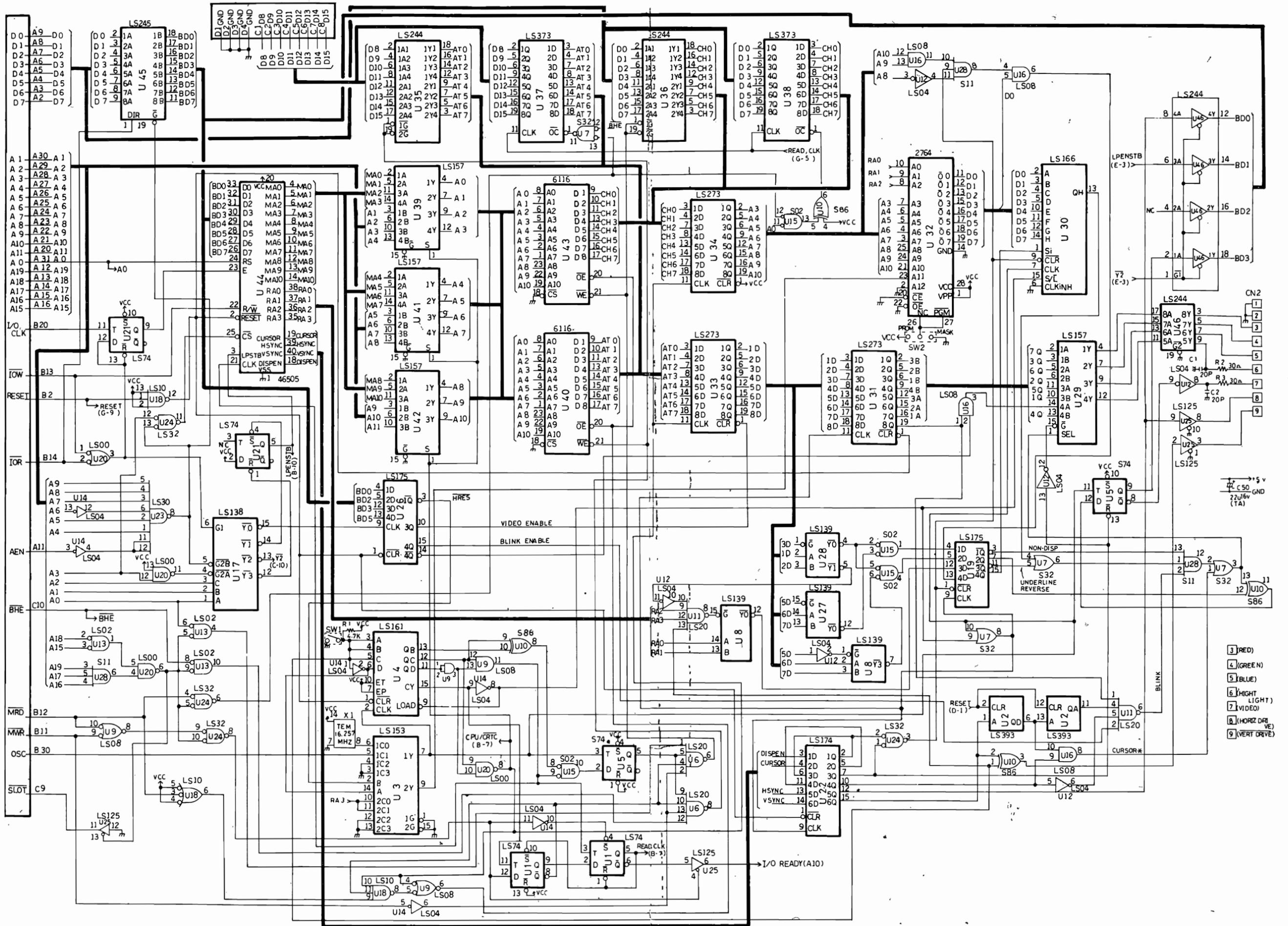
SUB BOARD



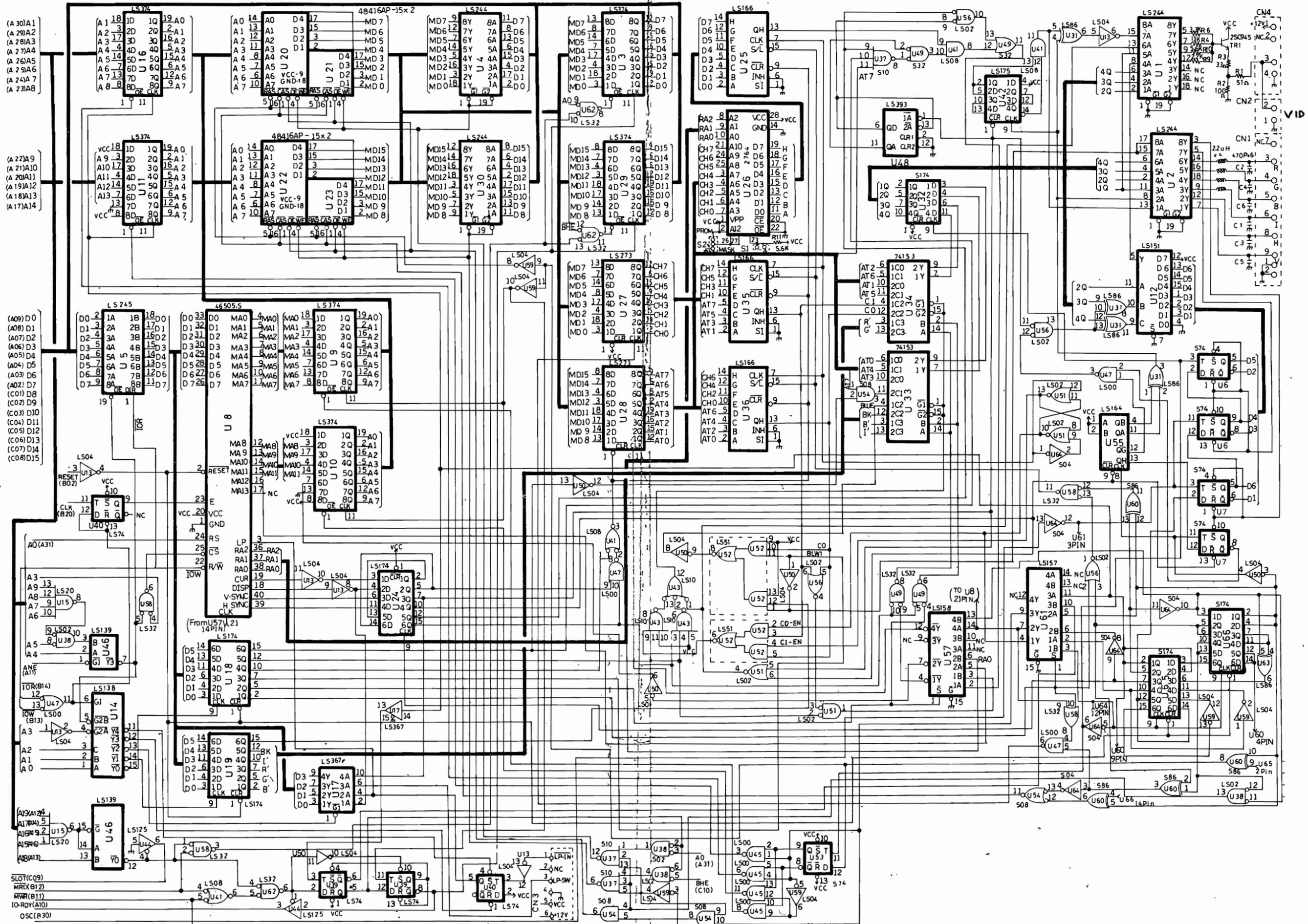
- TR1 2SA1357(Y)
- TR3 2SC2655(Y)
- TR3 2SC3262

Marked with "*"...Applicable Serial Nos. are 23125~ and 43125~.
Marked with "(")"...Changed part No.

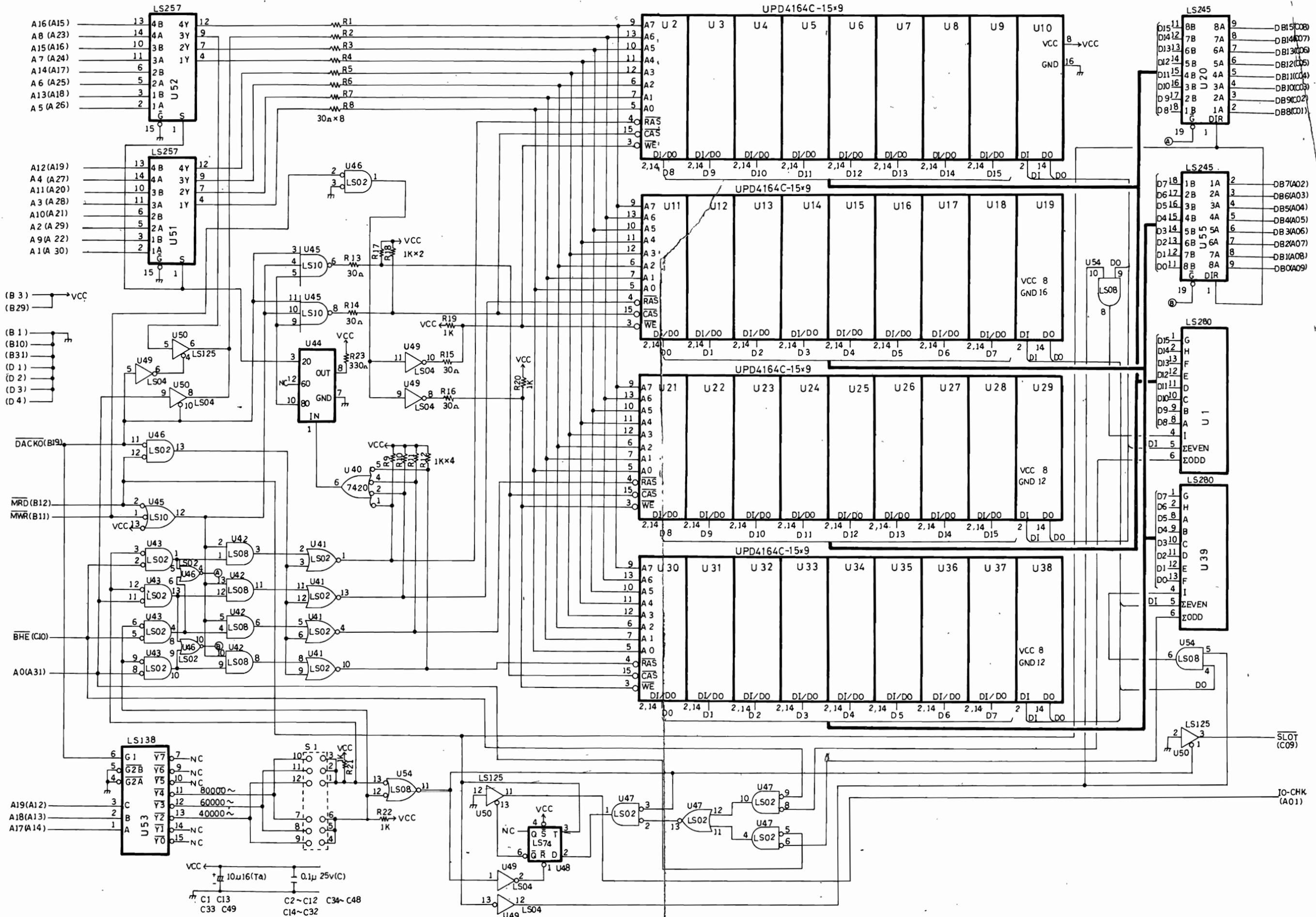
IX-2.5. Monochrome Display Adapter Board



IX-2-6. Color Display Adapter Board



IX-2-7. RAM Board



PART X

APPENDIX

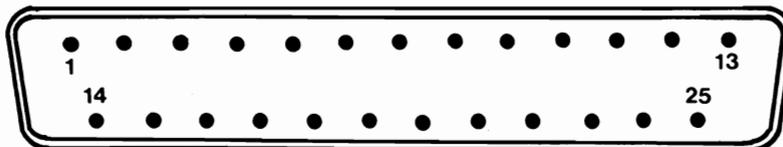
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X-1. Connector Pin Assignment

X-1-1. RS-232C Interface

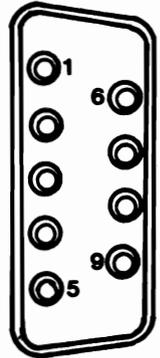
Pin No.	Description	Input/Output
1	Not Used	
2	Transmit Data	Output
3	Receive Data	Input
4	Request To Send	Output
5	Clear To Send	Input
6	Data Set Ready	Input
7	Signal Ground	
8	Carrier Detect	Input
9	Not Used	
10	Not Used	
11	Not Used	
12	Not Used	
13	Not Used	
14	Not Used	
15	Not Used	
16	Not Used	
17	Not Used	
18	Not Used	
19	Not Used	
20	Data Terminal Ready	Output
21	Not Used	
22	Ring Indicate	Input
23	Not Used	
24	Not Used	
25	Not Used	



MALE PINS

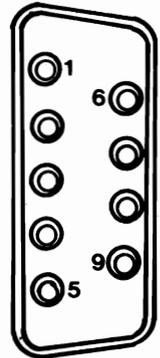
X-1-2. Monochrome Monitor Interface

Pin No.	Description	Input/Output
1	Ground	
2	Ground	
3	Not Used	
4	Not Used	
5	Not Used	
6	Intensity	Output
7	Video	Output
8	Horizontal	Output
9	Vartical	Output



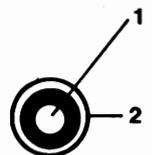
X-1-3. Color Monitor Interface

Pin No.	Description	Input/Output
1	Ground	
2	Ground	
3	Red	Output
4	Green	Output
5	Blue	Output
6	Intensity	Output
7	Reserved	Output
8	Horizontal	Output
9	Vartical	Output



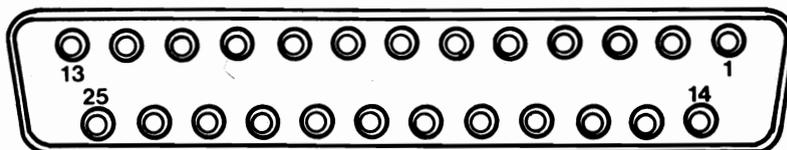
X-1-4. Video Composit Interface

Pin No.	Description	Input/Output
1	Composit Signal	Output
2	Ground	



X-1-5. Printer Interface

Pin No.	Description	Input/Output
1	$\overline{\text{Strobe}}$	Output
2	Data Bit 0	Output
3	Data Bit 1	Output
4	Data Bit 2	Output
5	Data Bit 3	Output
6	Data Bit 4	Output
7	Data Bit 5	Output
8	Data Bit 6	Output
9	Data Bit 7	Output
10	$\overline{\text{Acknowledge}}$	Input
11	Busy	Input
12	Paper End	Input
13	Select	Input
14	$\overline{\text{Auto Feed}}$	Output
15	$\overline{\text{Error}}$	Input
16	$\overline{\text{Initialize Printer}}$	Output
17	$\overline{\text{Select Input}}$	Output
18	Ground	
19	Ground	
20	Ground	
21	Ground	
22	Ground	
23	Ground	
24	Ground	
25	Ground	



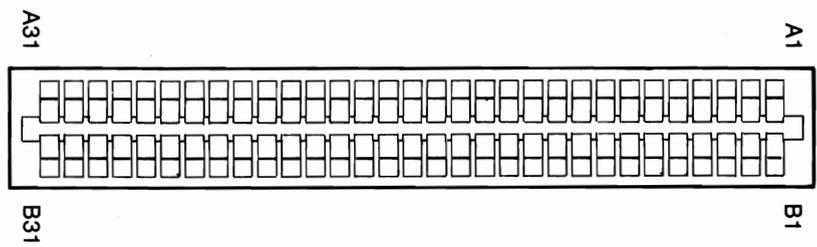
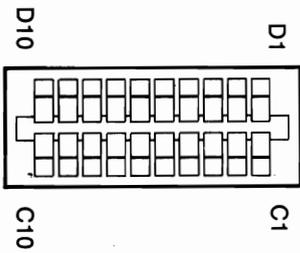
X-1-6. Option Slot Interface

Pin No.	Description	Input/Output
A01	$\overline{\text{IOCHK}}$	Input
A02	D7	Input/Output
A03	D6	Input/Output
A04	D5	Input/Output
A05	D4	Input/Output
A06	D3	Input/Output
A07	D2	Input/Output
A08	D1	Input/Output
A09	D0	Input/Output
A10	IORDY	Input
A11	AEN	Output
A12	A19	Output
A13	A18	Output
A14	A17	Output
A15	A16	Output
A16	A15	Output
A17	A14	Output
A18	A13	Output
A19	A12	Output
A20	A11	Output
A21	A10	Output
A22	A9	Output
A23	A8	Output
A24	A7	Output
A25	A6	Output
A26	A5	Output
A27	A4	Output
A28	A3	Output
A29	A2	Output
A30	A1	Output
A31	A0	Output

Pin No.	Description	Input/Output
B01	Ground	
B02	RESET	Output
B03	+5V	
B04	IRQ2	Input
B05	Not Used	
B06	Not Used	
B07	-12V	
B08	$\overline{\text{HRQIO}}$	Input
B09	+12V	
B10	Ground	
B11	$\overline{\text{MWR}}$	Output
B12	$\overline{\text{MRD}}$	Output
B13	$\overline{\text{IOW}}$	Output
B14	$\overline{\text{IOR}}$	Output
B15	$\overline{\text{DACK3}}$	Output
B16	DREQ3	Input
B17	$\overline{\text{DACK1}}$	Output
B18	DREQ1	Input
B19	$\overline{\text{DACK0}}$	Output
B20	CLK	Output
B21	IRQ7	Input
B22	Not Used	
B23	IQR5	Input
B24	IRQ4	Input
B25	IQR3	Input
B26	Not Used	
B27	Not Used	
B28	ALE	Output
B29	+5V	
B30	OSC	Output
B31	Ground	

C01	D8	Input/Output
C02	D9	Input/Output
C03	D10	Input/Output
C04	D11	Input/Output
C05	D12	Input/Output
C06	D13	Input/Output
C07	D14	Input/Output
C08	D15	Input/Output
C09	$\overline{\text{SLOT}}$	Input
C10	$\overline{\text{BHE}}$	Output

D01	Ground
D02	Ground
D03	Ground
D04	Ground
D05	Not Used
D06	Not Used
D07	Not Used
D08	Not Used
D09	Not Used
D10	Not Used



X-2. Character Code Table

Decimal	Hexadecimal	Character
0	00	BLANK (NULL)
1	01	☺
2	02	●
3	03	♥
4	04	♦
5	05	♣
6	06	♠
7	07	
8	08	◻
9	09	
10	0A	
11	0B	
12	0C	
13	0D	
14	0E	♪
15	0F	♁
16	10	▶
17	11	◀
18	12	↕
19	13	!!
20	14	π
21	15	§
22	16	■
23	17	↕
24	18	↑
25	19	↓
26	1A	→
27	1B	←
28	1C	
29	1D	
30	1E	
31	1F	
32	20	BLANK (SPACE)
33	21	!
34	22	"
35	23	#
36	24	\$
37	25	%
38	26	&
39	27	'
40	28	(
41	29)
42	2A	*
43	2B	+
44	2C	,
45	2D	-
46	2E	.
47	2F	/

Decimal	Hexadecimal	Character
48	30	0
49	31	1
50	32	2
51	33	3
52	34	4
53	35	5
54	36	6
55	37	7
56	38	8
57	39	9
58	3A	:
59	3B	;
60	3C	<
61	3D	=
62	3E	>
63	3F	?
64	40	@
65	41	A
66	42	B
67	43	C
68	44	D
69	45	E
70	46	F
71	47	G
72	48	H
73	49	I
74	4A	J
75	4B	K
76	4C	L
77	4D	M
78	4E	N
79	4F	O
80	50	P
81	51	Q
82	52	R
83	53	S
84	54	T
85	55	U
86	56	V
87	57	W
88	58	X
89	59	Y
90	5A	Z
91	5B	[
92	5C	\
93	5D]
94	5E	^
95	5F	_

Decimal	Hexadecimal	Character
96	60	`
97	61	a
98	62	b
99	63	c
100	64	d
101	65	e
102	66	f
103	67	g
104	68	h
105	69	i
106	6A	j
107	6B	k
108	6C	l
109	6D	m
110	6E	n
111	6F	o
112	70	p
113	71	q
114	72	r
115	73	s
116	74	t
117	75	u
118	76	v
119	77	w
120	78	x
121	79	y
122	7A	z
123	7B	{
124	7C	
125	7D	}
126	7E	~
127	7F	△
128	80	Ç
129	81	ü
130	82	é
131	83	â
132	84	ä
133	85	à
134	86	å
135	87	ç
136	88	ê
137	89	ë
138	8A	è
139	8B	ï
140	8C	î
141	8D	ì
142	8E	À
143	8F	Ä

Decimal	Hexadecimal	Character
144	90	Ē
145	91	æ
146	92	Æ
147	93	ô
148	94	ö
149	95	ò
150	96	û
151	97	ù
152	98	ÿ
153	99	Ö
154	9A	Ü
155	9B	ç
156	9C	£
157	9D	¥
158	9E	Pt
159	9F	ƒ
160	A0	á
161	A1	í
162	A2	ó
163	A3	ú
164	A4	ñ
165	A5	Ñ
166	A6	ª
167	A7	º
168	A8	¿
169	A9	¬
170	AA	¬
171	AB	½
172	AC	¼
173	AD	ı
174	AE	<<
175	AF	>>
176	B0	⋮
177	B1	⋮
178	B2	⋮
179	B3	□
180	B4	▣
181	B5	▣
182	B6	▣
183	B7	▣
184	B8	▣
185	B9	▣
186	BA	▣
187	BB	▣
188	BC	▣
189	BD	▣
190	BE	▣
191	BF	▣
192	C0	▣

Decimal	Hexadecimal	Character
193	C1	▣
194	C2	▣
195	C3	▣
196	C4	▣
197	C5	▣
198	C6	▣
199	C7	▣
200	C8	▣
201	C9	▣
202	CA	▣
203	CB	▣
204	CC	▣
205	CD	▣
206	CE	▣
207	CF	▣
208	D0	▣
209	D1	▣
210	D2	▣
211	D3	▣
212	D4	▣
213	D5	▣
214	D6	▣
215	D7	▣
216	D8	▣
217	D9	▣
218	DA	▣
219	DB	■
220	DC	■
221	DD	■
222	DE	■
223	DF	■
224	E0	α
225	E1	β
226	E2	Γ
227	E3	π
228	E4	Σ
229	E5	σ
230	E6	μ
231	E7	τ
232	E8	ϕ
233	E9	θ
234	EA	Ω
235	EB	δ
236	EC	∞
237	ED	φ
238	EE	€
239	EF	∩
240	F0	≡
241	F1	±

Decimal	Hexadecimal	Character
242	F2	≥
243	F3	≤
244	F4	∫
245	F5	∫
246	F6	÷
247	F7	≈
248	F8	○
249	F9	●
250	FA	●
251	FB	√
252	FC	n
253	FD	2
254	FE	█
255	FF	BLANK FF

Canon