MCM6256B

256K-Bit Dynamic RAM

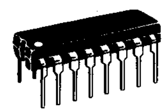
The MCM6256B is a 262,144 bit, high-speed, dynamic random access memory. Organized as 262,144 one-bit words and fabricated using N-channel silicon-gate MOS technology, this single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. All inputs and outputs are fully TTL compatible.

By multiplexing row and column address inputs, the MCM6256B requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

The MCM6256B features "page mode" which allows random column accesses of the 512 bits within the selected row.

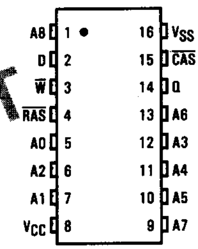
- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (±10%)
- Maximum Access Time: MCM6256B-10 = 100 ns
  MCM6256B-12 = 120 ns
  MCM6256B-15 = 150 ns
- Low Power Dissipation: MCM6256B-10 = 440 mW Maximum (Active)
  MCM6256B-12 = 396 mW Maximum (Active)
  MCM6256B-15 = 358 mW Maximum (Active)
  28 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{RAS}$-Only Refresh Mode
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- Page Mode Capability

TO BE PHASED OUT IN 1989



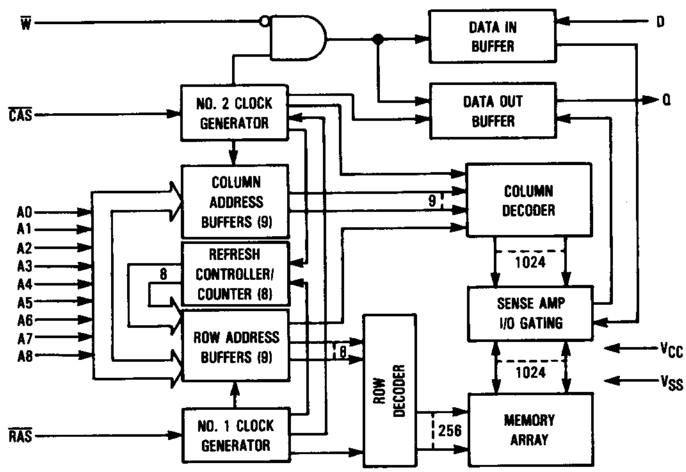
P PACKAGE
PLASTIC
CASE 648D

PIN ASSIGNMENT



PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM6256B-10, t_{RC} = 190 ns		—	80		
MCM6256B-12, t_{RC} = 220 ns		—	72		
MCM6256B-15, t_{RC} = 260 ns		—	65		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	5.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM6256B-10, t_{RC} = 190 ns		—	70		
MCM6256B-12, t_{RC} = 220 ns		—	62		
MCM6256B-15, t_{RC} = 260 ns		—	55		
V_{CC} Power Supply Current During Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM6256B-10, t_{PC} = 100 ns		—	60		
MCM6256B-12, t_{PC} = 120 ns		—	55		
MCM6256B-15, t_{PC} = 145 ns		—	50		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh	I_{CC5}			mA	2
MCM6256B-10, t_{RC} = 190 ns		—	70		
MCM6256B-12, t_{RC} = 220 ns		—	62		
MCM6256B-15, t_{RC} = 260 ns		—	55		
Input Leakage Current ($V_{SS} < V_{in} < V_{CC}$)	$I_{lkg(I)}$	−10	10	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} < V_{out} < V_{CC}$)	$I_{lkg(O)}$	−10	10	µA	
Output Logic 1 Voltage (I_{out} = −5 mA)	V_{OH}	2.4	—	V	
Output Logic 0 Voltage (I_{out} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit	Notes
Input Capacitance	A0-A8, D	C_{in}	—	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		—	7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	—	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 5)

Parameter	Symbol		MCM6256B-10		MCM6256B-12		MCM6256B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	190	—	220	—	260	—	ns	4, 5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	200	—	240	—	285	—	ns	4, 5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	220	—	260	—	310	—	ns	4, 5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	100	—	120	—	150	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	50	—	60	—	75	ns	7, 8
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	5	25	5	30	5	35	ns	9
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	80	—	90	—	100	—	ns	—
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	—
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	—
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	50	25	60	25	75	ns	10
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	—
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	—	15	—	15	—	ns	—
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	—
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	—	25	—	30	—	ns	—
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	70	—	85	—	105	—	ns	—
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	—
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	—
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	11
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	—	15	—	20	—	ns	11
Write Command Hold Time	t_{CELWH}	t_{WCH}	20	—	25	—	30	—	ns	—
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	70	—	85	—	105	—	ns	—
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	—	25	—	30	—	ns	—
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	25	—	35	—	45	—	ns	—
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	25	—	35	—	45	—	ns	—
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	12
Data in Hold Time	t_{CELDX}	t_{DH}	20	—	25	—	30	—	ns	12
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	70	—	85	—	105	—	ns	—
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	10	—	ns	—
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	50	—	60	—	75	—	ns	—
Refresh Period	t_{RVRV}	t_{RFSH}	—	4	—	4	—	4	ms	—

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
5. AC measurements t_T = 5.0 ns.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

2

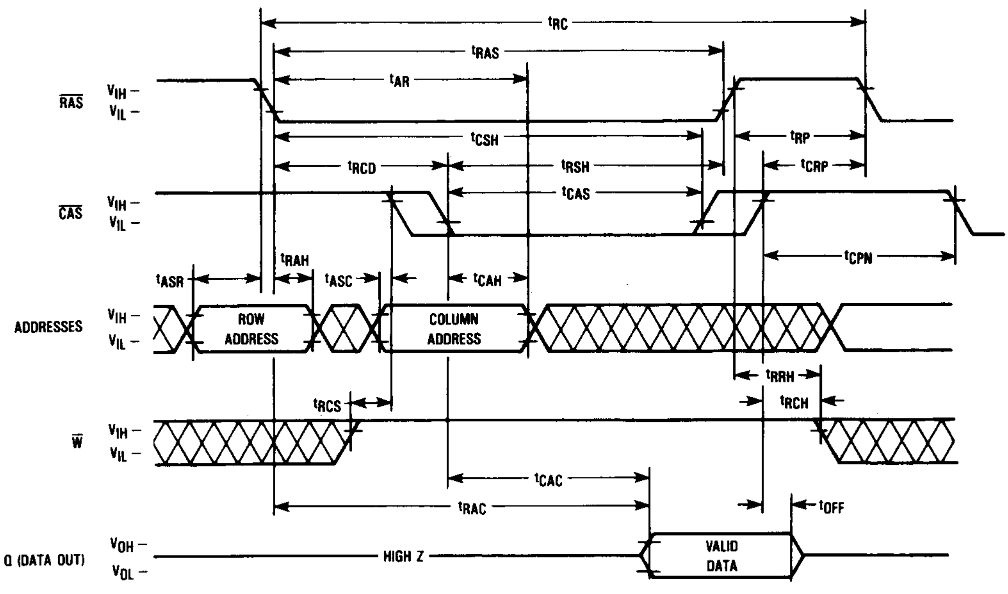
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM6256B-10		MCM6256B-12		MCM6256B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	13
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	30	—	40	—	50	—	ns	13
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	80	—	100	—	125	—	ns	13
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	100	—	120	—	150	—	ns	—
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	—	20	—	25	—	ns	—
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	40	—	50	—	60	—	ns	—
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	100	—	120	—	145	—	ns	—
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	110	—	140	—	170	—	ns	—
Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRMW}	130	—	160	—	195	—	ns	—
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	—	30	—	30	—	ns	—
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	—	10	—	10	—	ns	—
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	—
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	—	50	—	60	—	ns	—

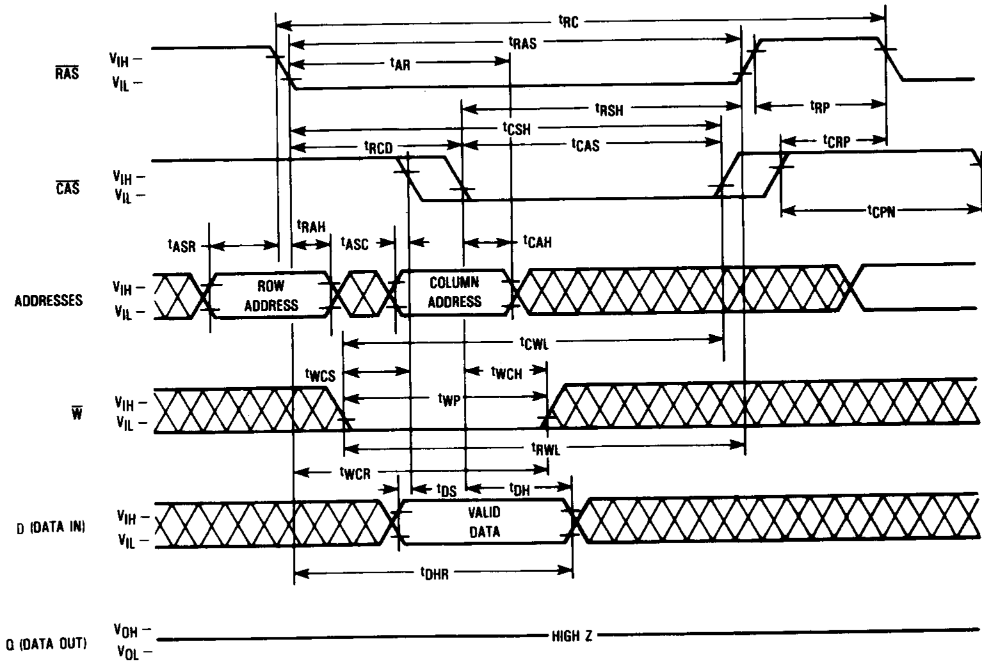
NOTES:

13. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

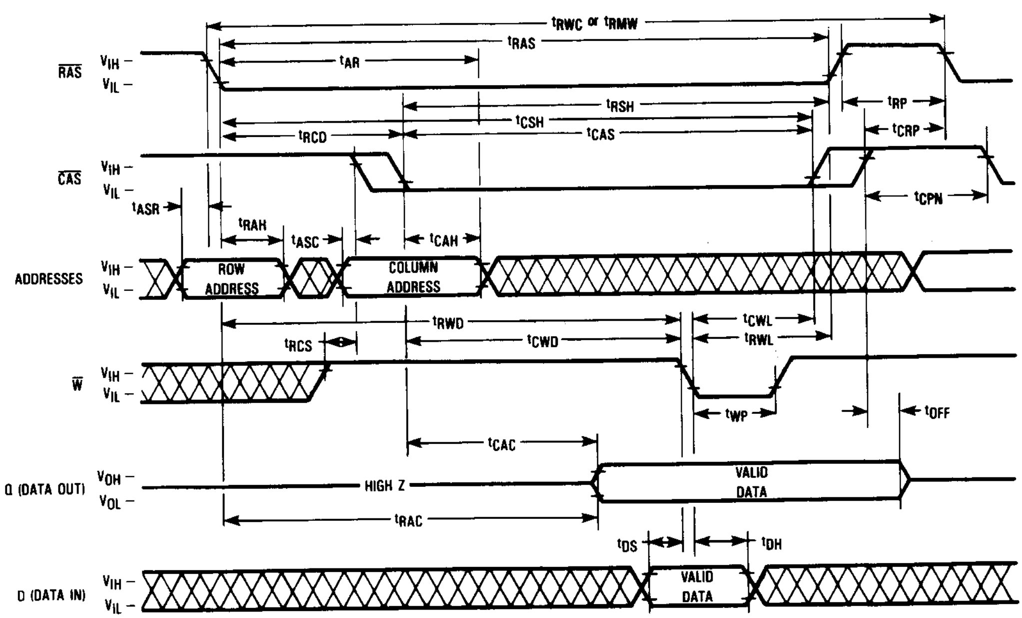
READ CYCLE TIMING



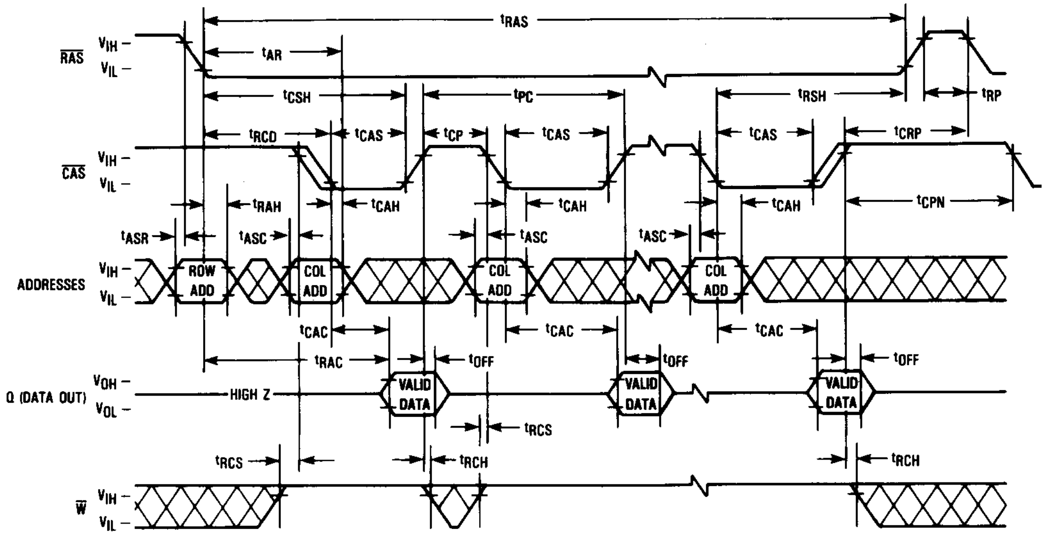
WRITE CYCLE TIMING



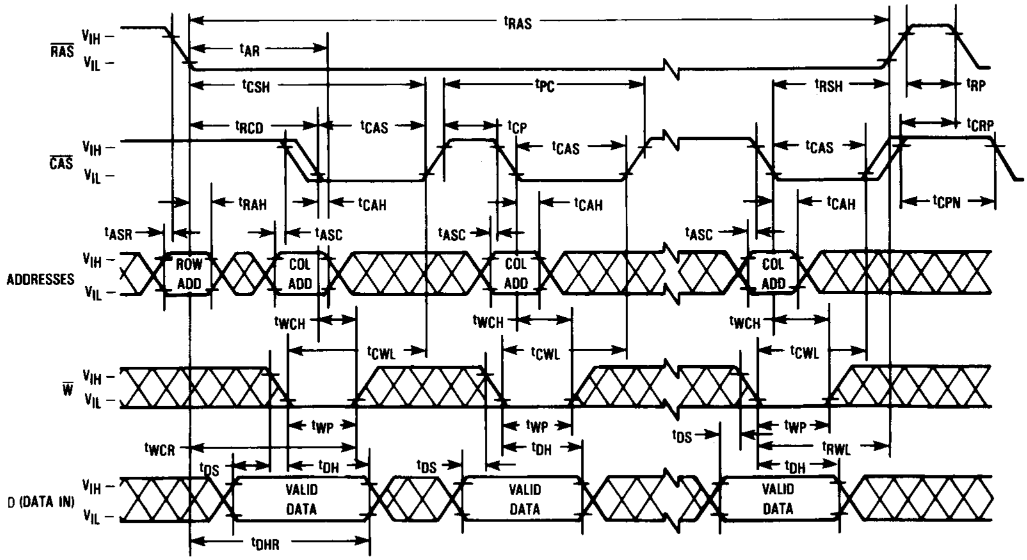
READ-WRITE/READ-MODIFY-WRITE CYCLE



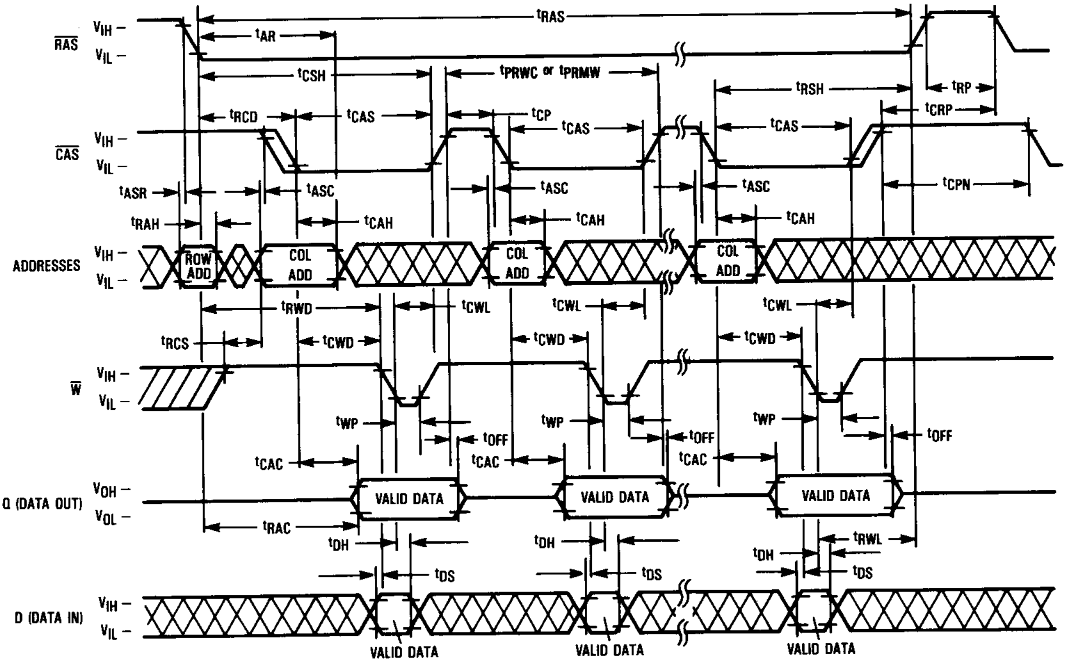
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

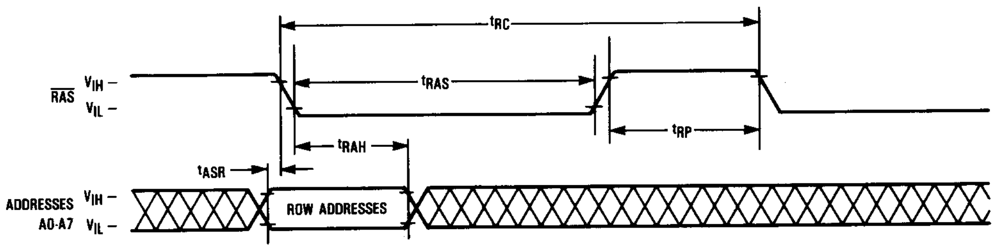


PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



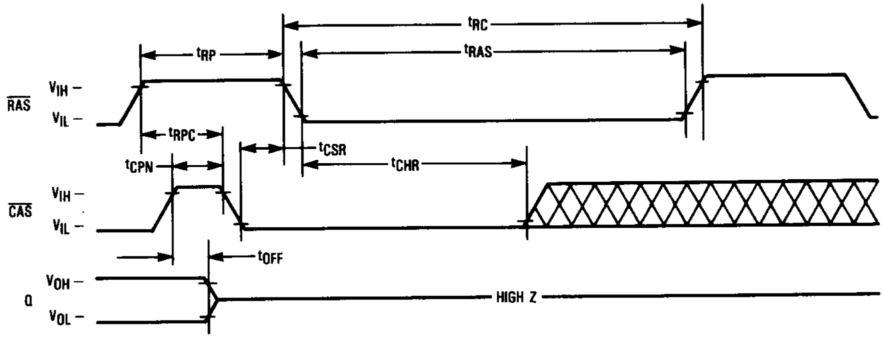
RAS-ONLY REFRESH CYCLE

(D, W, and A8 are Don't Care, CAS is High)



CAS-BEFORE RAS REFRESH CYCLE

(W, D, and A0-A8 are Don't Care)



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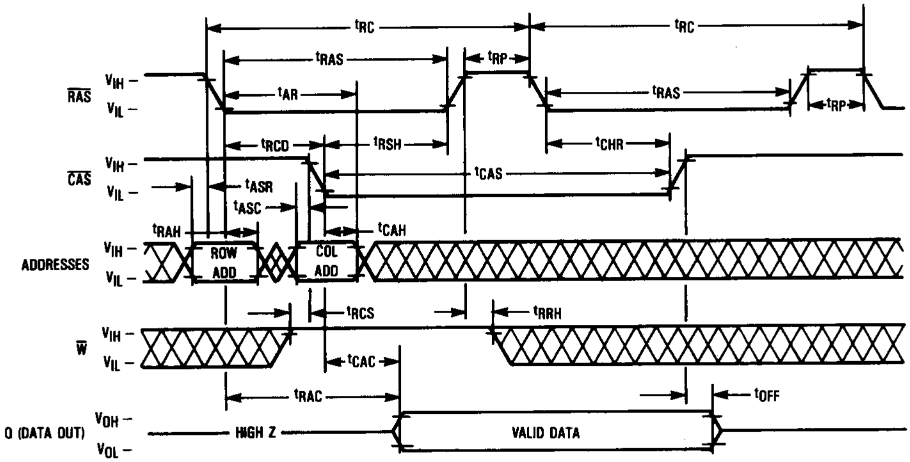
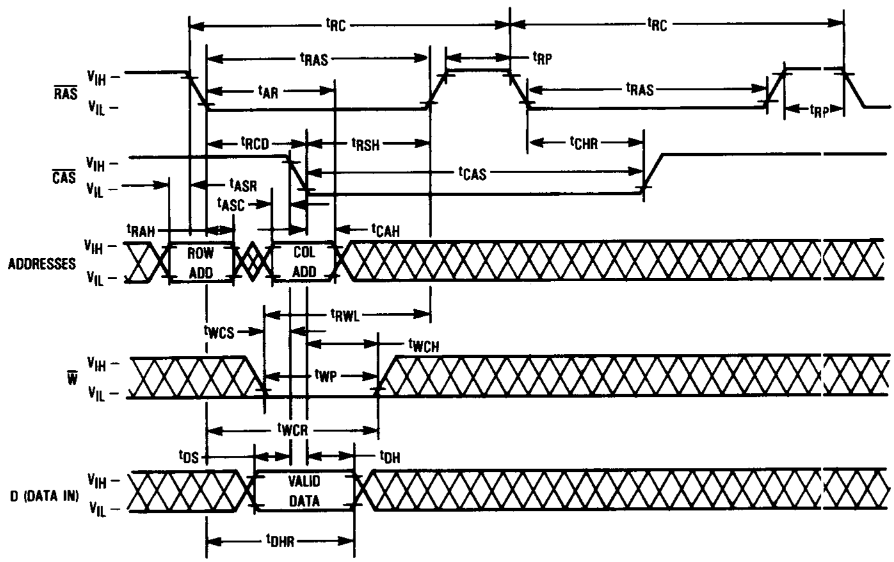
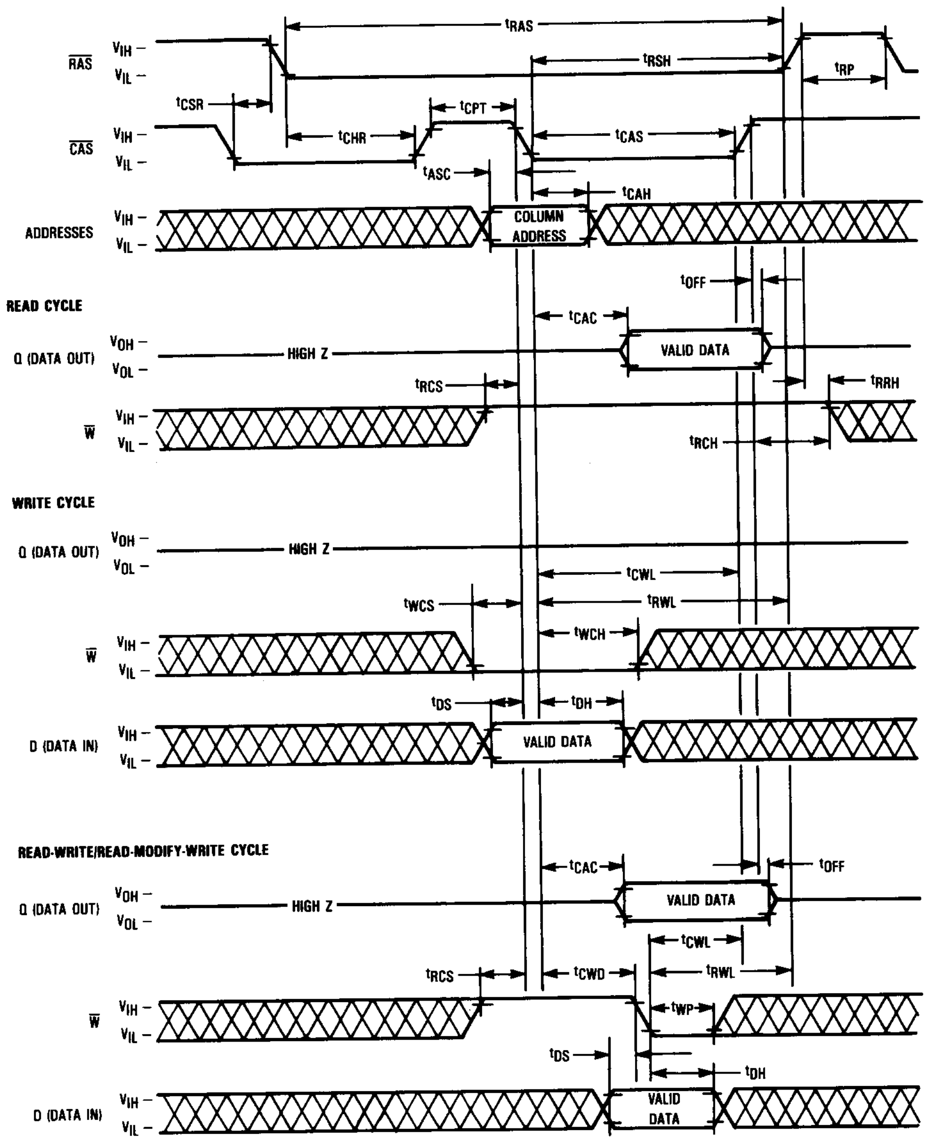
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 256K RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where an 8-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A8 (pin 1) is not required for refresh. The other variation, which is called page mode, allows the user to column access the 512 bits within a selected row. (See **PAGE-MODE CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at the 512 column locations on a given row. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 256K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 9-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 milliseconds. This is accomplished by sequentially cycling through the 256 row address locations every 4 milliseconds, (i.e., at least one row every 15.6 microseconds like the 64K dynamic RAM). A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 256 row addresses every 4 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM6256B can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

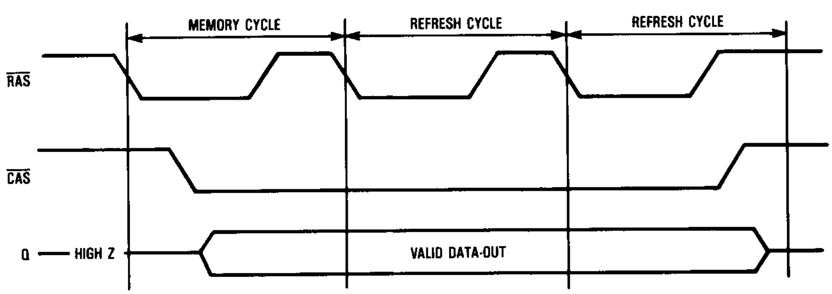


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)

MCM 6256B X XX

- Motorola Memory Prefix — MCM
- Part Number — 6256B
- Package (P = Plastic) — X
- Speed (10 = 100 ns, 12 = 120 ns, 15 = 150 ns) — XX

Full Part Numbers — MCM6256BP10
MCM6256BP12
MCM6256BP15