Personal Computer Hardware Reference Library

IBM Personal Computer Data Acquisition and Control Adapter Technical Reference

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Contents

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Description

The IBM Personal Computer Data Acquisition and Control Adapter (Data Acquisition Adapter) provides both analog and digital I/O capabilities. It is installed in any full-length expansion slot, and up to four may be installed in a system.

The adapter provides:

- Four analog input channels multiplexed into an analog-to-digital converter (ADC), with 12-bit resolution
- Two analog output channels, each having its own digital-to-analog converter (DAC), with 12-bit resolution
- A 16-bit digital input port
- A 16-bit digital output port
- A 32-bit timer
- A 16-bit, externally-clocked, timer/counter
- An expansion bus.

The Data Acquisition Adapter has a 16-bit data bus and a buffered 8-bit data bus.

The adapter's 16-bit data bus provides access to:

- An analog I/O device:
  - Analog input subsystem with four multiplexed channels
  - Analog output subsystem with two DACs
- A binary I/O device:
  - 16-bit digital input port
  - 16-bit digital output port
  - Handshaking
- An expansion bus.

The buffered 8-bit data bus provides access to:

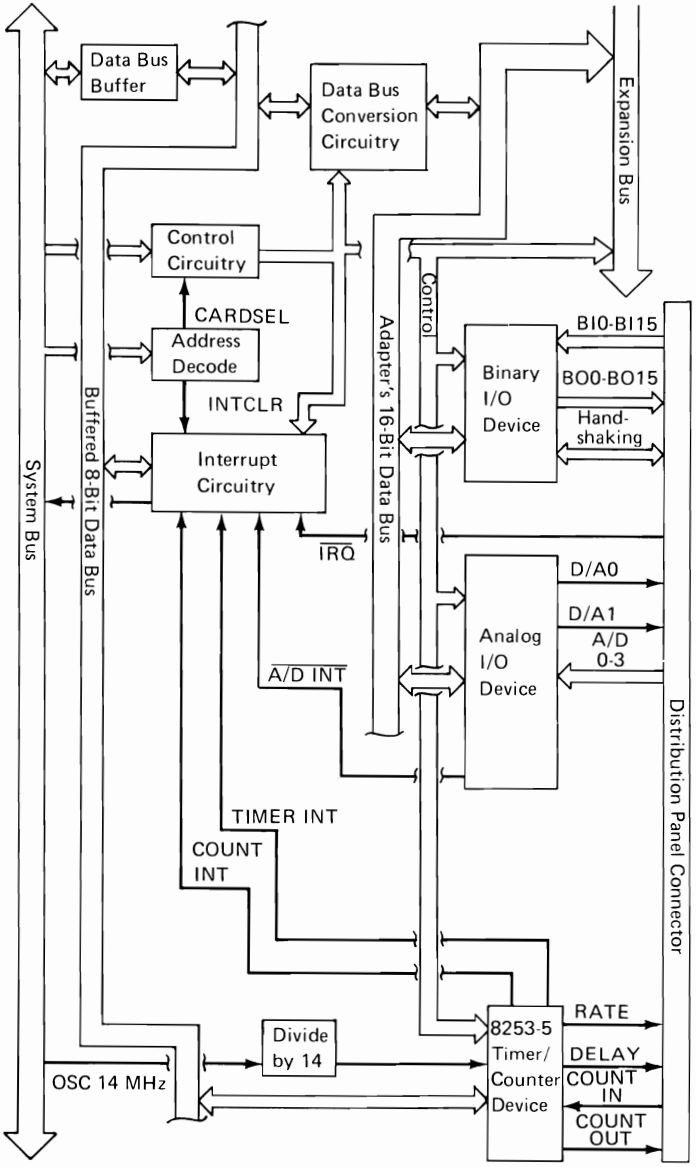
- Interrupt circuitry
- A timer/counter device:
  - 32-bit timer (Counters 0 and 1)
  - 16-bit timer/counter (Counter 2).

Low and high bytes are transferred between the adapter's buffered 8-bit data bus and 16-bit data bus.

A 60-pin, distribution-panel connector is provided for external access to the analog I/O device, the binary I/O device, and the timer/counter device.

Major Components

Following is a block diagram of the Data Acquisition Adapter.



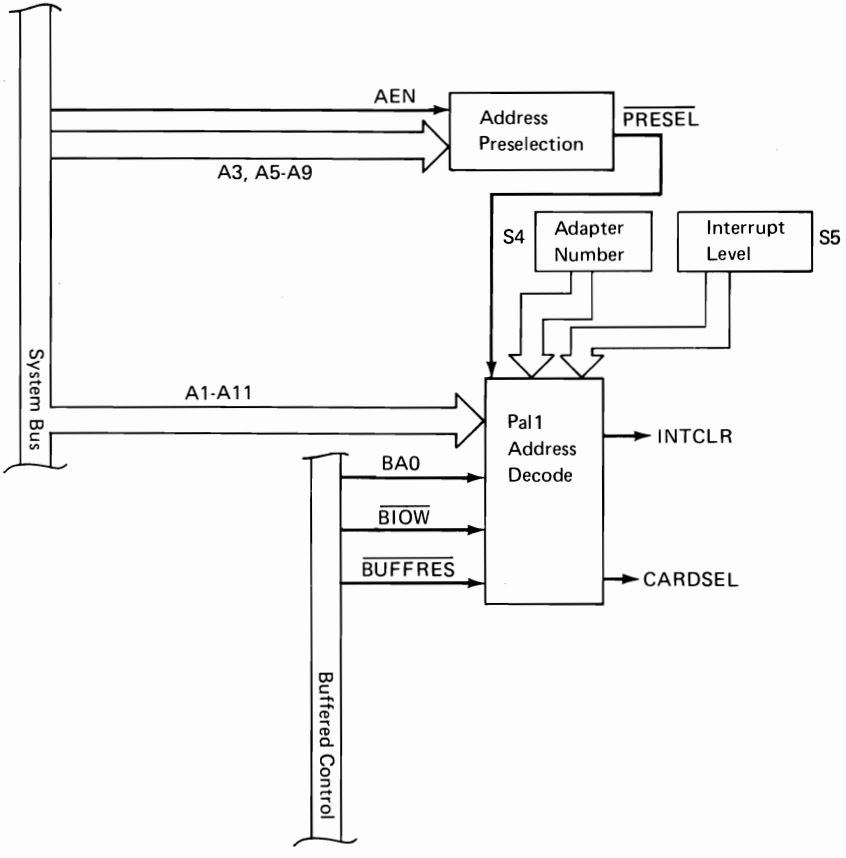
The following are descriptions of the major components shown in the figure on the previous page.

Address Decode and Control Circuitry

The following are descriptions of address decode and control circuitry.

Address Decode

Following is a block diagram of address decode.



The signals used by the address decode circuitry are:

AEN Address enable: De-gates the processor and other devices from the I/O channel to allow direct-memory access (DMA) transfers to take place. When active (high), the DMA controller has control of the address bus, data bus, read command lines (memory and I/O), and the write command lines (memory and I/O).

$\overline{\text{PRESEL}}$ Preselect: Indicates preliminary address decoding of the 'address enable' signal (AEN), and the address bits that are common to the adapter's base address and to the shared-interrupt address.

CARDSEL Card select: Indicates communication is in process between the Data Acquisition Adapter and the system. The shared-interrupt re-activation function is not included.

INTCLR Shared-interrupt reactivation control signal.

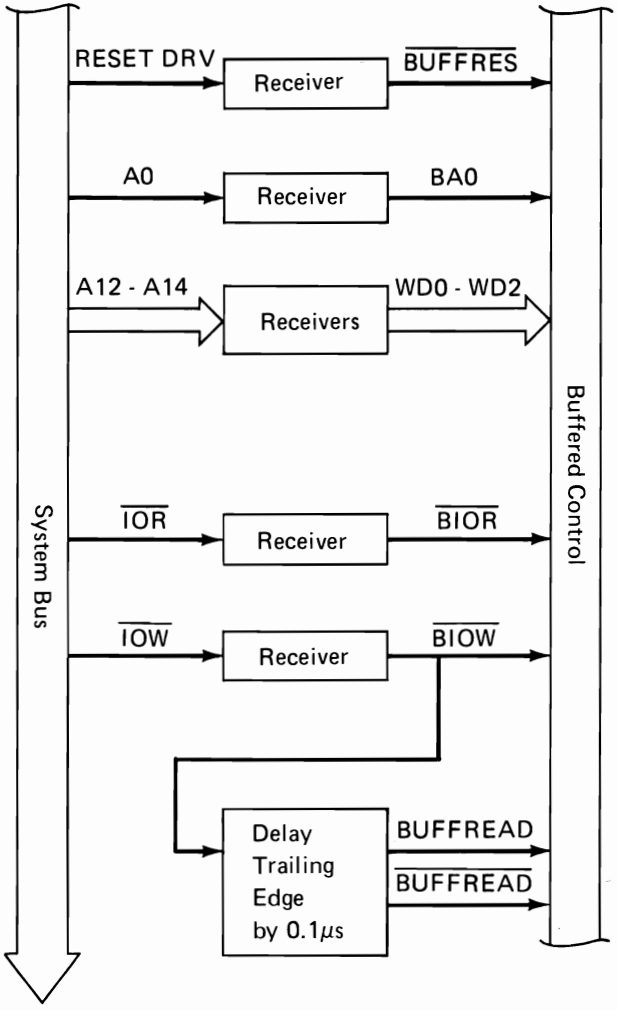
The address preselection circuitry decodes the six address lines, which are common in the adapter address and the shared-interrupt address. AEN is used to prevent false decodes during DMA cycles. Because the adapter has a base address of hex 2E2 through 2E3, and the shared-interrupt address is hex 02Fx (where x is shared-interrupt level 3, 4, 5, 6, or 7), the common address bits are: A9, A7, A6, and A5 equal to 1, and A8 and A3 equal to 0. The resulting signal ($\overline{\text{PRESEL}}$) indicates that either an adapter access or a shared-interrupt access may be occurring.

The address decode circuitry uses the signals $\overline{\text{PRESEL}}$, A10, A11, A4, and the signals from the switches S4-1 and S4-2 to decode an adapter's base address. The control decode circuitry uses the resulting signal (CARDSEL) as a master enable and then generates the individual control signals.

When the address decoded is hex 2Fx (where x is the shared interrupt level), INTCLR is generated. INTCLR reactivates the adapter's interrupt circuitry. The address decode circuitry also generates an INTCLR signal at power-on-reset time. Power-on-reset occurs when the 'buffer reset' signal ($\overline{\text{BUFFRES}}$), which is created by the system bus signal (RESET DRV), goes low.

System Bus Address and Control Signals

The following is a block diagram of the address and control signals from the system bus.



The address and control signals from the system bus are as follows:

RESET DRV — Resets system logic upon power-on or during a low line-voltage outage. RESET DRV is synchronized to the falling edge of 'clock' and is active high.

$\overline{\text{BUFFRES}}$ — Buffer reset: Inverse of RESET DRV. Provides power-on-reset of the adapter's control logic. $\overline{\text{BUFFRES}}$ is active low.

WD0 - WD2 — Word number bits 0 through 2 (system bus address lines A12 through A14 are buffered and renamed WD0 through WD2). Selects word registers 0 through 7 when system bus address line A15 is low. Selects word registers 8 through 15 when A15 is high.

BA0 — Buffered system-bus address line A0: Selects high or low bytes.

$\overline{\text{BIOR}}$ — Buffered I/O read ($\overline{\text{IOR}}$): $\overline{\text{BIOR}}$ is active low and is used for I/O read operations on the buffered 8-bit data bus.

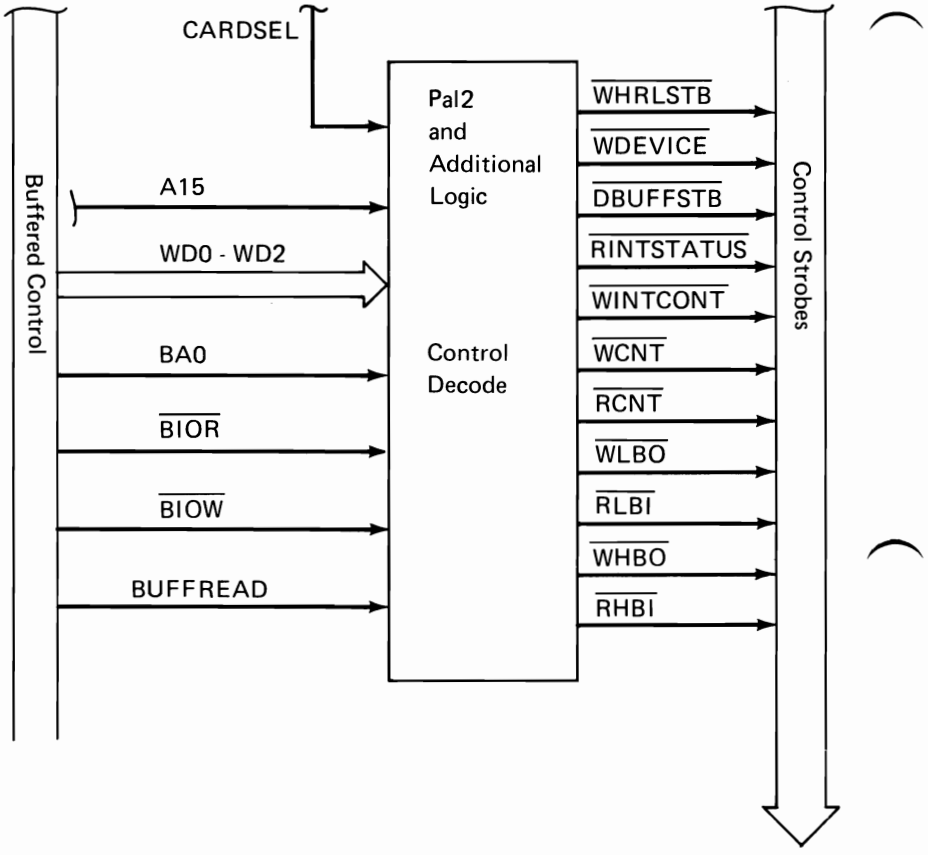
$\overline{\text{BIOW}}$ — Buffered I/O write($\overline{\text{IOW}}$): $\overline{\text{BIOW}}$ is active low and is used for I/O write operations on the buffered 8-bit data bus.

BUFFREAD Buffer read: Indicates whether a read or a write operation on the adapter's 16-bit data bus is to be performed. When high, this signal indicates a read operation, and when it is low, a write operation is indicated.

$\overline{\text{BUFFREAD}}$ Inverse of BUFFREAD.

Control Decode

Following is a block diagram of the control decode circuitry.



The control decode circuitry inputs CARDSEL, A15, WD0 through WD2, BA0, $\overline{\text{BIOR}}$, $\overline{\text{BIOW}}$, and BUFFREAD generate the following control strobes:

$\overline{\text{WHRLSTB}}$ Write-high read-low strobe: Strobe for reading or writing the data word from the adapter's 16-bit data bus to an on-board or expansion device.

$\overline{\text{WDEVICE}}$ Write device: Write strobe for the on-board or expansion device number register.

$\overline{\text{DBUFFSTB}}$ Data buffer strobe: Enable strobe for data communications between the system bus and the Data Acquisition Adapter.

$\overline{\text{RINTSTATUS}}$ Read interrupt status: Read strobe for the interrupt status register.

$\overline{\text{WINTCONT}}$ Write interrupt control: Write strobe for the interrupt status register.

$\overline{\text{WCNT}}$ Write counter: Write strobe for the timer/counter.

$\overline{\text{RCNT}}$ Read counter: Read strobe for the timer/counter.

$\overline{\text{WLBO}}$ Write low byte out: Latch control strobe for latching the low data byte for later transmission to an on-board or expansion device.

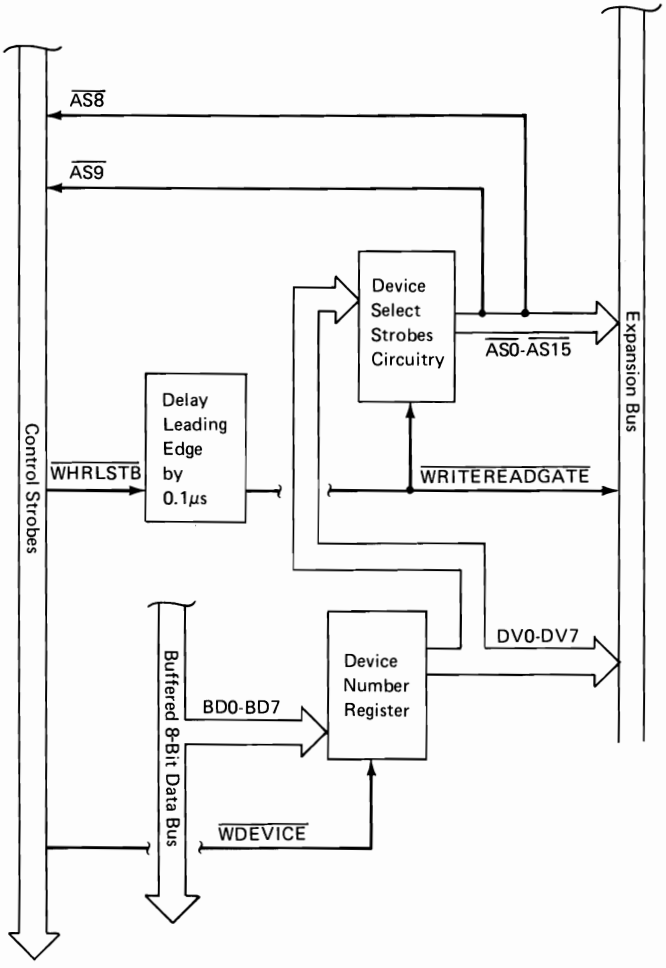
$\overline{\text{RLBI}}$ Read low byte in: Enable strobe for reading a data word from an on-board or expansion device to the adapter's 16-bit data bus. The low byte is transmitted to the system bus during this strobe. The high byte is latched during $\overline{\text{RLBI}}$ for later transmission to the system bus.

$\overline{\text{WHBO}}$ Write high byte out: Enable strobe for writing a data word from the adapter's 16-bit data bus to an on-board or expansion device. The low byte is the one previously latched in $\overline{\text{WLBO}}$. The high byte is the current data from the system bus.

$\overline{\text{RHBI}}$ Read high byte in: Enable strobe for reading the high byte (previously latched by $\overline{\text{RLBI}}$) from the adapter's 16-bit data bus to the system bus.

Device Selection

The following figure shows the device selection circuitry.



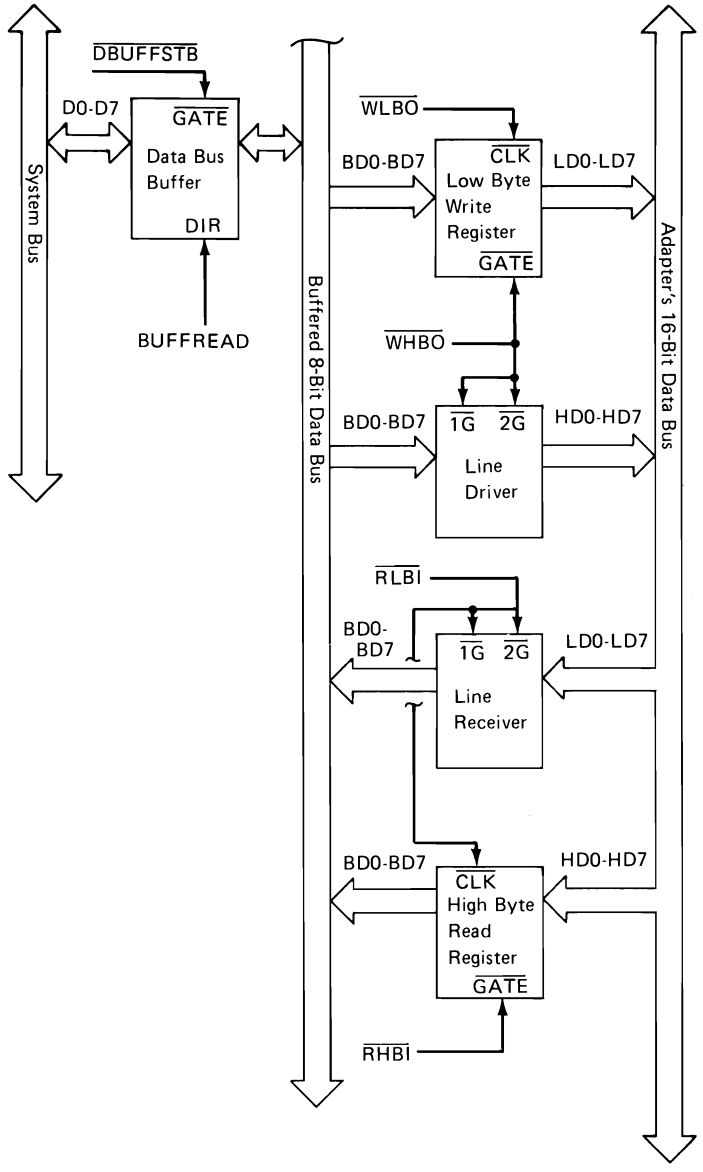
The device number register stores the device number. Device strobes are generated for on-board and expansion devices.

The following are used for device selection:

DV0 - DV7	Device number register bits 0 through 7
$\overline{\text{WRITEREADGATE}}$	Strobe for all devices
$\overline{\text{AS0}}$ through $\overline{\text{AS15}}$	Strobes for devices 0 through 15: $\overline{\text{AS8}}$ selects the binary I/O device, and $\overline{\text{AS9}}$ selects the analog I/O device.

Data Bus Conversion Circuitry

Following is a block diagram of the data bus conversion circuitry.



Data Bus Buffer

The system's data bus (D0 through D7) is buffered by the data bus buffer to create the adapter's buffered data bus (BD0 through BD7). The data bus buffer is activated by $\overline{\text{DBUFFSTB}}$ during all communications between the system bus and the Data Acquisition Adapter. The data direction is determined by BUFFREAD.

The buffered 8-bit data bus is used for direct 8-bit data communication with the interrupt circuitry, the timer/counter device, and the device number register.

The buffered 8-bit data bus also communicates with the low byte write register, a line driver, a line receiver, and the high byte read register to implement the conversion of the buffered 8-bit data bus into the adapter's 16-bit data bus.

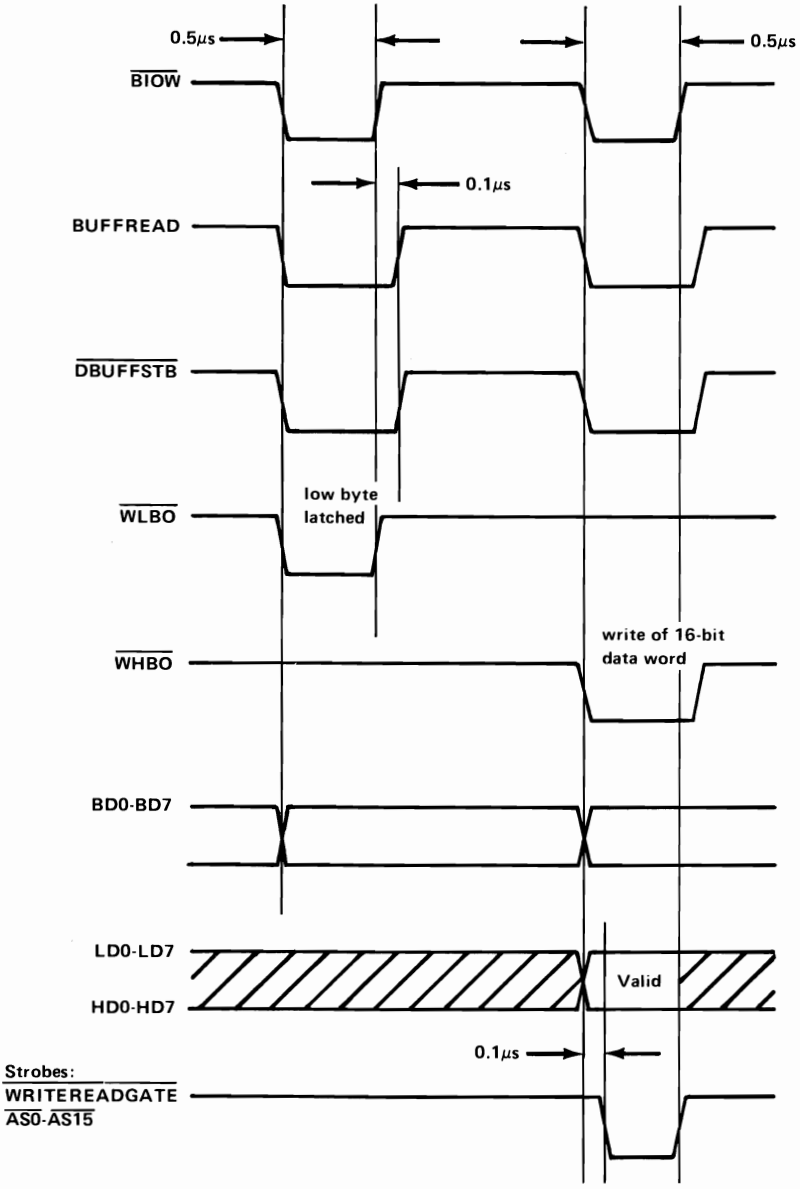
Writing Data

Data is written sequentially from the system data bus to the adapter's 16-bit data bus. The low byte is first written to an even address, then the high byte is written to an odd address. The entire 16-bit word is transmitted to an on-board or expansion device at the same time that the high byte is written.

When data is written from the system data bus to an even address (A0 is 0), the $\overline{\text{WLBO}}$ (write low byte out) strobe occurs. The low-byte write register latches the data.

When data is written from the system data bus to an odd address (A0 is 1), the $\overline{\text{WHBO}}$ (write high byte out) strobe occurs. The low-byte write register transmits the previously latched low byte to the adapter's 16-bit data bus LD lines, 0 through 7. At the same time, the line driver transmits the current data on the buffered 8-bit data bus BD lines, 0 through 7, to the adapter's 16-bit data bus HD lines, 0 through 7.

Following is a write timing diagram of the adapter's 16-bit data bus.



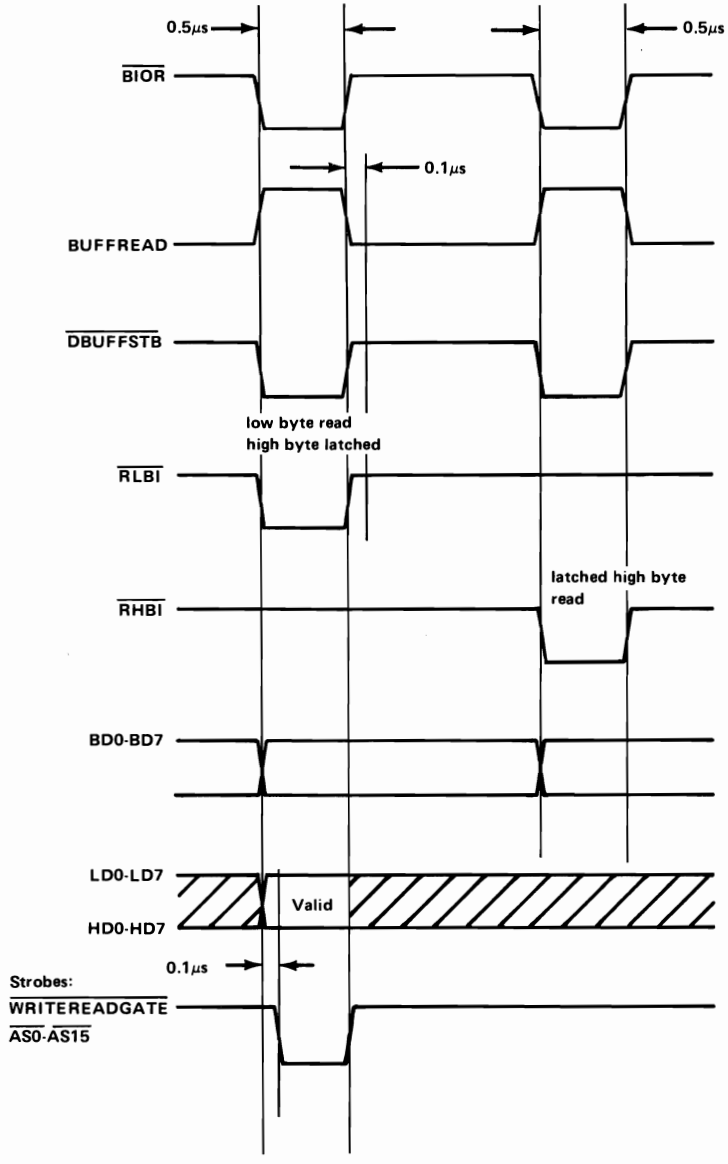
Reading Data

Data is read sequentially from the adapter's 16-bit data bus to the system data bus. The low data byte is first read at an even address, then the high data byte is read at an odd address. The entire 16-bit word is transmitted from an on-board or expansion device at the same time that the low byte is read.

When data is read to the system data bus at an even address (A0 is 0), the $\overline{\text{RLBI}}$ (read low byte in) strobe occurs. The line receiver transmits the low byte from the adapter's 16-bit data bus LD lines, 0 through 7, to the system data bus. At the same time, the high-byte read register latches the data from the adapter's 16-bit data bus HD lines, 0 through 7.

When data is read from the system data bus at an odd address (A0 is 1), the $\overline{\text{RHBI}}$ strobe occurs. The high-byte read register transmits the previously latched high byte to the system data bus.

Following is a read timing diagram of the adapter's 16-bit data bus.



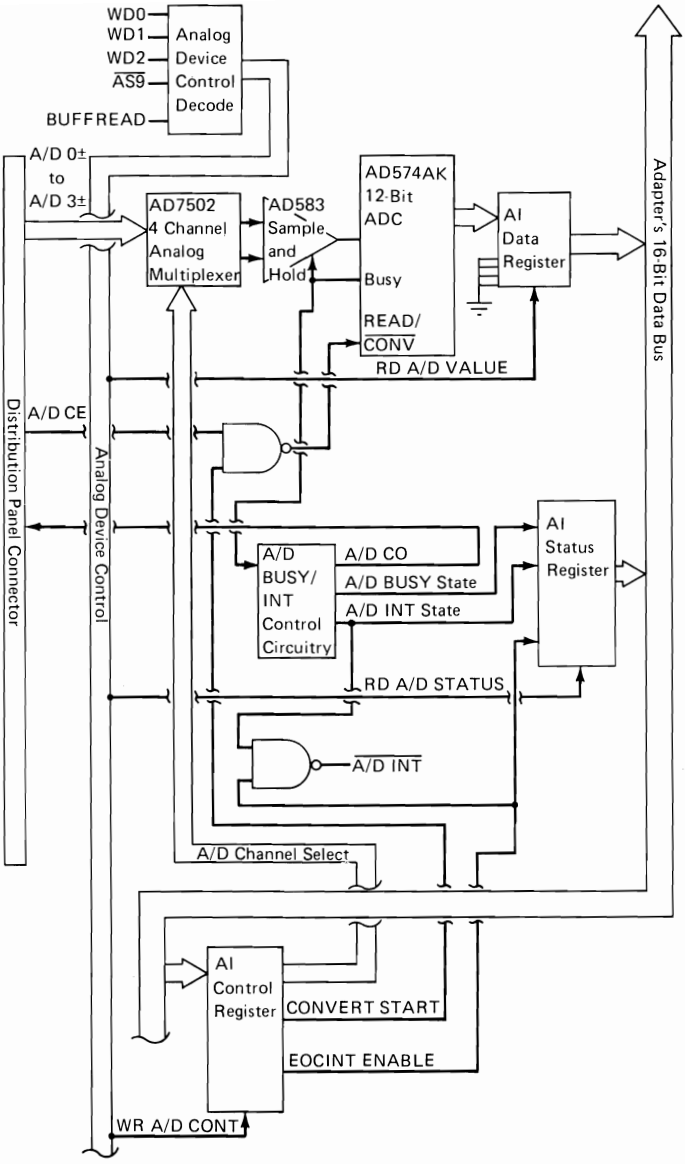
Analog I/O Device

The Data Acquisition Adapter's analog I/O device consists of two subsystems:

- Analog input: An analog-to-digital conversion subsystem.
- Analog output: A digital-to-analog conversion subsystem.

Analog Input Subsystem

On the following page is a block diagram of the analog input subsystem.



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Analog-to-digital conversion is the process of converting analog signals (voltages) over a given range to digital values.

Unlike digital (binary) signals, which have only two voltage states, analog signals have infinite voltage levels over a particular range.

Analog-to-digital converters (ADCs) are categorized by the number of bits of resolution they allow. The greater the number of bits, the greater the number of discrete voltage levels that can be represented.

The Data Acquisition Adapter has an analog input device with the following features:

- Four, multiplexed, differential channels
- An ADC with 12-bit resolution
- Switch-selectable ranges
- Optional data-conversion control with 'A/D convert out' and 'A/D convert enable in' lines.

The Data Acquisition Adapter's analog input device (device number 9) has four channels, which are multiplexed into a single ADC. This device converts analog signals in one of three ranges to digital values in the range of 0 to 4095.

The three switch-selectable ranges are:

- - 5 to +5 volts
- -10 to +10 volts
- 0 to +10 volts

The relationship of the analog input voltage to the returned digital value depends on the range for which the hardware is configured. The selected range setting for analog input is in effect for all analog input channels. For example, in the -5 to +5 volt configuration, an input of +4.997 volts generates a full-scale value of 4095; an input of 0 volts generates a value of 2048; and an input of -5 volts generates a value of 0.

Analog Input Device Control

The use of the $\overline{AS9}$ strobe causes the analog input device to be accessed as device number 9.

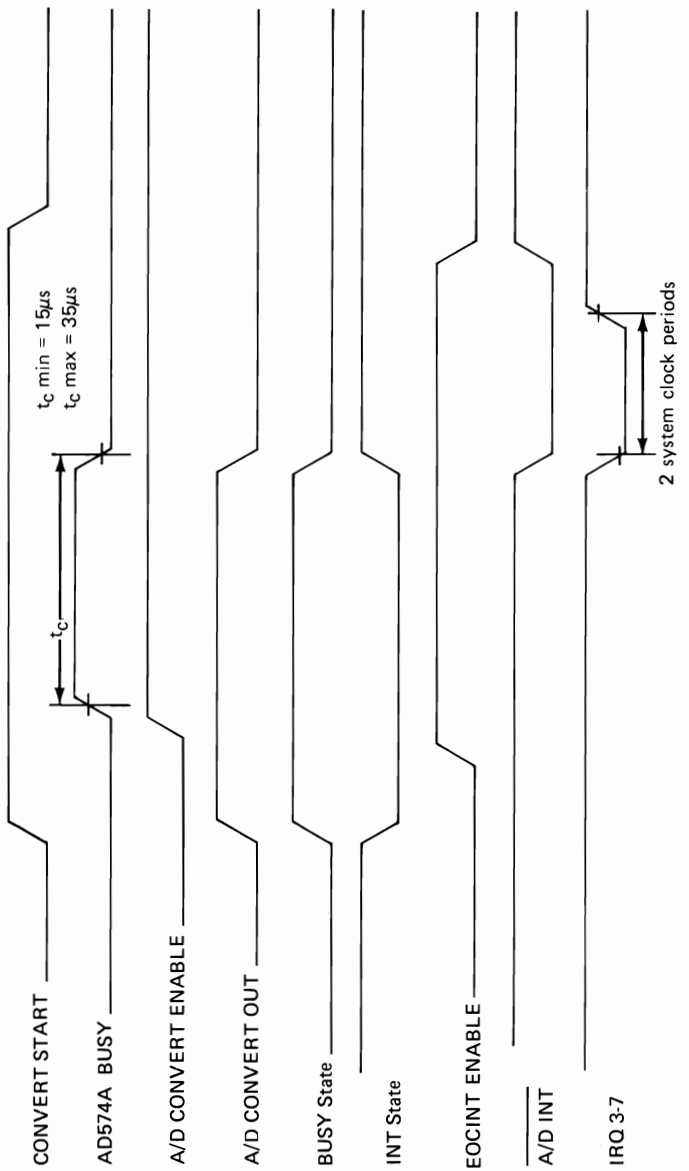
The control decode circuitry of the analog device decodes WD0 through WD2, $\overline{AS9}$, and BUFFREAD to generate the following control signals:

WR A/D CONT	Write analog-to-digital control. Allows the AI control register to be written to.
RD A/D STATUS	Read analog-to-digital status. Allows reading of the AI status register.
RD A/D VALUE	Read analog-to-digital value. Allows reading of the AI data register.

Analog Input Device Registers

AI Control Register	The AI control register contains the analog-to-digital channel selection, analog-to-digital interrupt-enable information, and convert start bit information. The AI control register is cleared by $\overline{BUFFRES}$ during power-on- reset.
AI Status Register	The AI status register contains information about 'A/D busy,' the 'A/D interrupt status,' and the readback of the 'A/D interrupt enable.'
AI Data Register	The 16-bit AI data register contains the data from the ADC. Because the output of the ADC is a 12-bit digital value, the four highest bits of the register are grounded.

Following is a timing diagram of analog-to-digital conversion.



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Starting an Analog-to-Digital Conversion

The convert start bit from the AI control register is logically ANDed with the external 'A/D convert enable' signal from the distribution panel connector. The result is inverted to generate an active low signal, which is brought to the READ/$\overline{\text{CONV}}$ pin of the AD574 ADC.

Reading an Analog-to-Digital Value

The READ/$\overline{\text{CONV}}$ pin must be taken high before the analog-to-digital value can be read. This is accomplished by writing a convert start bit equal to 0 to the AI control register.

Channel Selection

The differential analog to digital channel pair is selected by the AD7502 4-channel, analog multiplexer on the basis of the analog-to-digital channel-select bits of the AI control register.

Sample and Hold

During a conversion, the 'busy' signal from the AD574A ADC causes the AD583 Sample and Hold to hold its present value when the 'busy' signal is high, and starts sampling again when it is low.

'A/D Busy' and Interrupt States

At the end of a conversion, the AD574 ADC's 'busy' signal goes low, and the AI status register shows that the analog input device is in the not-busy and interrupting state.

'A/D Interrupt'

The actual 'A/D interrupt' signal (A/D INT) is a result of the logical ANDing of the INT STATE status bit in the AI status register, and the EOCINT ENABLE bit from the AI control register. The inverted result generates $\overline{\text{A/D INT}}$ (an active low signal), which goes to the interrupt circuitry.

'A/D Convert Out'

The 'A/D convert out' (A/D CO) signal is brought out to the distribution panel connector on the Data Acquisition Adapter.

The 'A/D convert out' signal is set (TTL high) when a conversion has been commanded by programming the convert start bit. The signal remains high until the conversion is complete. If the analog signals received by the on-board analog input device are from an external device that can be made to send data on receipt of a TTL high pulse, you may use a synchronization scheme in which the program's request for an analog-to-digital conversion triggers (using 'A/D convert out') the output of analog data from the external device.

'A/D Convert Enable'

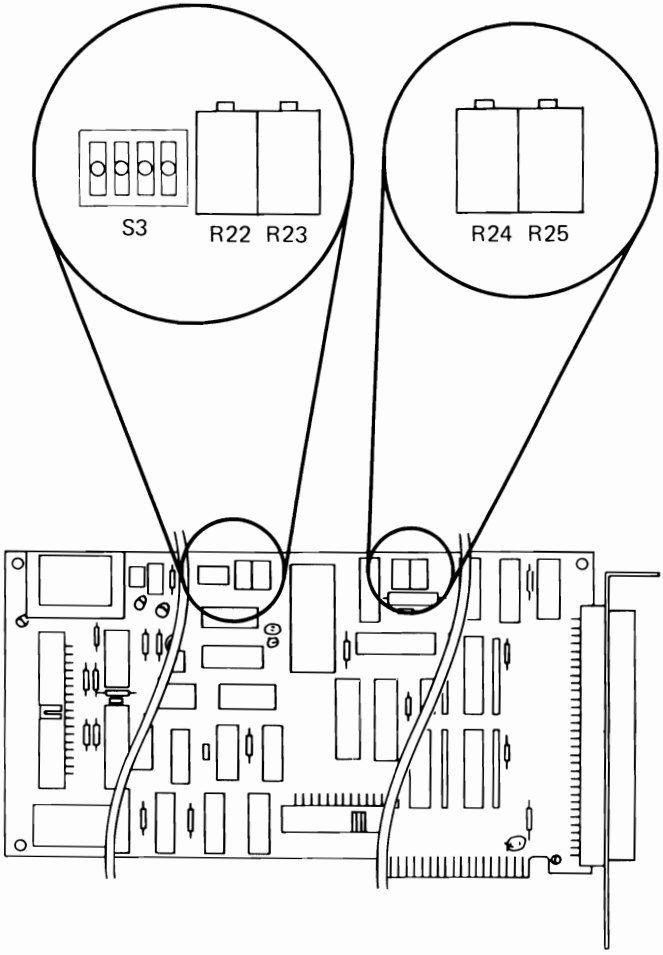
The 'A/D convert enable' (A/D CE) signal is brought out to the distribution panel connector on the Data Acquisition Adapter.

By holding the 'convert enable in' signal low (TTL), an external device can inhibit or delay all analog-to-digital conversions ordered by programming.

To be considered valid and allow an analog-to-digital conversion, the 'convert enable in' signal must remain high until the 'convert out' signal goes low again.

Analog Input Potentiometers

Four potentiometers (R22, R23, R24, and R25) on the Data Acquisition Adapter control bipolar offset, unipolar offset, gain, and common mode rejection for the analog input device. The following diagram shows the location of these potentiometers.



In the following "LSB" represents the weight of the least-significant bit of the 12-bit digital output code of the ADC.

The table shows the 1-LSB values for each analog input range.

Range	1 LSB
0 to +10 volts	2.44 mV
-5 to +5 volts	2.44 mV
-10 to +10 volts	4.88 mV

The ADC is intended to have a 1/2-LSB offset so the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). The information under "Bipolar Offset" and "Unipolar Offset" explains this 1/2-LSB offset.

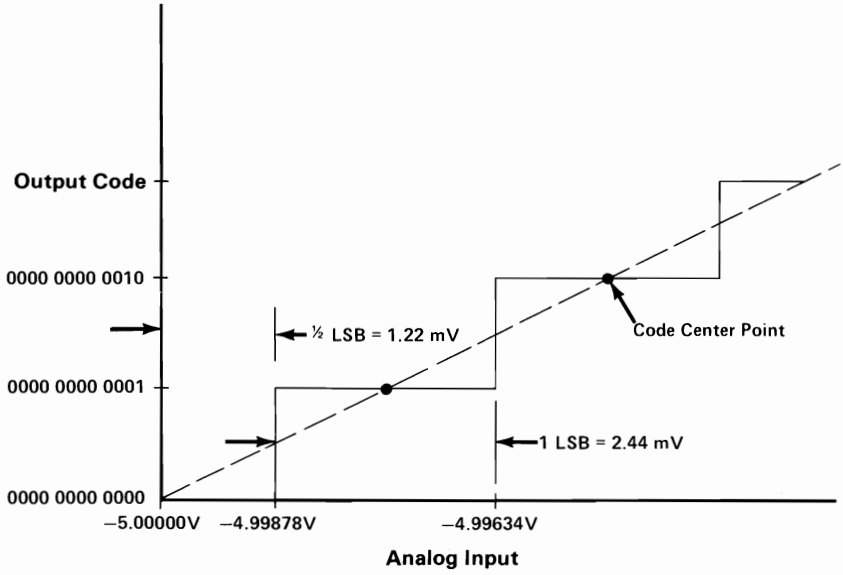
Bipolar Offset:

The value of R22 is set so the transition from the digital output code 0000 0000 0000 to 0000 0000 0001 occurs for an input voltage 1/2 LSB above negative full scale. R22 takes effect when a bipolar range (-5 to +5 volts or -10 to +10 volts) is selected.

The following shows the input voltages for the transition from the output code 0000 0000 0000 to 0000 0000 0001.

Range	Input Voltage for First Code Transition
-5 to +5 volts	-4.99878 volts
-10 to +10 volts	-9.99756 volts

The following shows the first few output-code transitions for the -5 to +5 volt range.



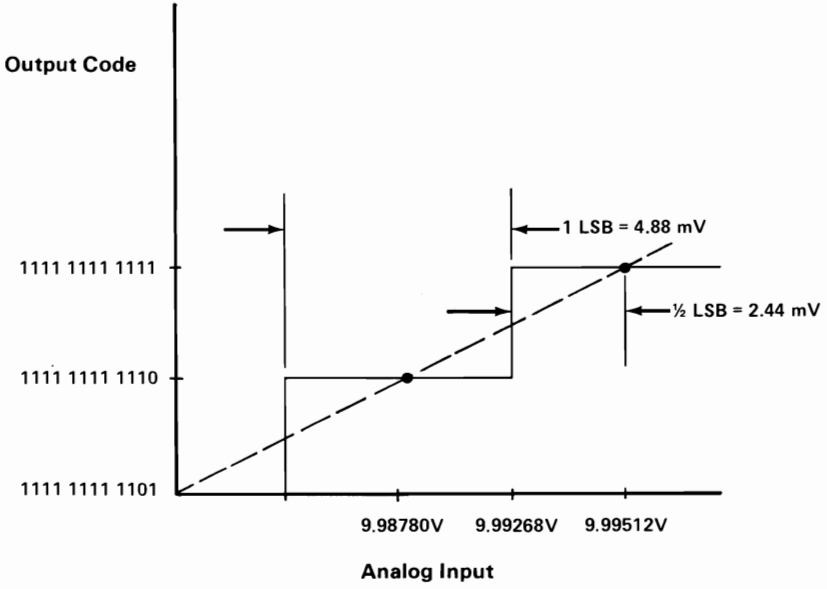
Gain:

The value of R23 is set so the last transition (1111 1111 1110 to 1111 1111 1111) occurs for an input voltage 1-1/2 LSB below full scale.

The following shows the input voltage for the transition from the output code 1111 1111 1110 to 1111 1111 1111.

Range	Input Voltage for Last Code Transition
0 to +10 volts	+9.99634 volts
-5 to +5 volts	+4.99634 volts
-10 to +10 volts	+9.99268 volts

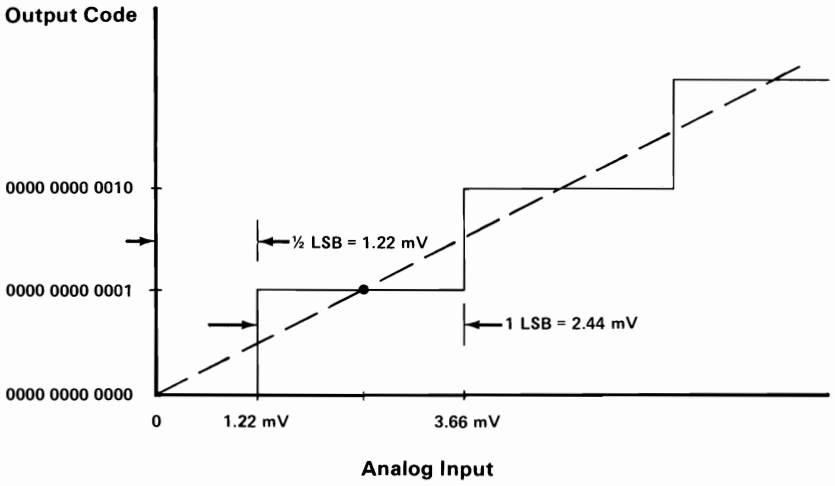
The following shows the last few output-code transitions for the -10 to +10 volt range.



Unipolar Offset:

The value of R24 is set so the first transition (0000 0000 0000 to 0000 0000 0001) occurs for an input voltage of +1/2 LSB. R24 takes effect when the unipolar range (0 to +10 volts) is selected.

The following shows the first few output-code transitions for the 0 to +10 volt range.

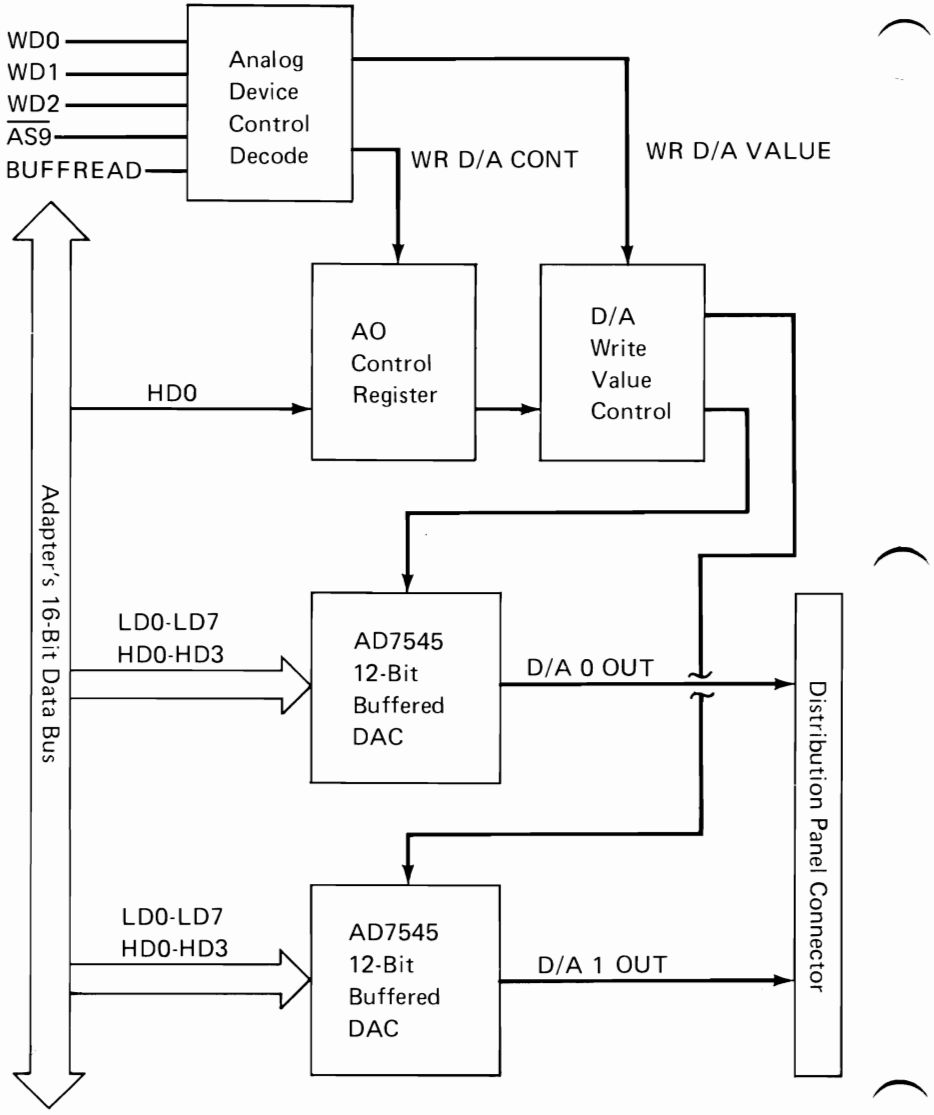


Common Mode Rejection:

R25 allows for the reduction and balancing of the error caused by common mode noise (voltage common to both sides of an analog input channel). The common-mode input range specification for the analog input device is ±11 volts maximum. The value of R25 is set so on the most sensitive range (-5 to +5 volts), the effect of common mode voltage is balanced on each side of zero volts. For example, a common mode voltage of +11 volts produces the same output code as a common mode voltage of -11 volts.

Analog Output Subsystem

Following is a block diagram of the analog output subsystem.



The Data Acquisition Adapter includes an on-board digital-to-analog output device with the following features:

- Two analog output channels, with each channel using separate DACs with 12-bit resolution
- Switch-selectable ranges for each converter

Each DAC converts digital values in the range of 0 to 4095 to voltages in one of three ranges. The switches on the adapter control voltage polarity and range.

The three switch-selectable ranges are:

- -5 to +5 volts
- -10 to +10 volts
- 0 to +10 volts

The settings of these switches determine the relationship between analog output values and the voltages from the analog output device. The relationship of the digital value to the analog output voltage depends on the range for which the hardware is configured. Because each analog output channel has its own DAC, the analog output range can be set for each channel. For example, in the 0 to +10 volt configuration, a digital value of 0 generates an output of 0 volts; a digital value of 2048 generates an output of +5 volts; and a digital value of 4095 generates an output of +9.997 volts.

Analog Output Device Control

The control decode circuitry of the analog device decodes WD0 through WD2, $\overline{AS9}$, and BUFFREAD to generate the following control signals:

WR D/A CONT — Write digital-to-analog control: Controls the writing of the channel-select bit to the AO control register. The channel-select bit is used to determine which digital-to-analog write strobe to generate.

WR D/A VALUE — Write digital-to-analog value: Controls the generation of the digital-to-analog write strobes. WR D/A VALUE occurs when the AO data register is addressed.

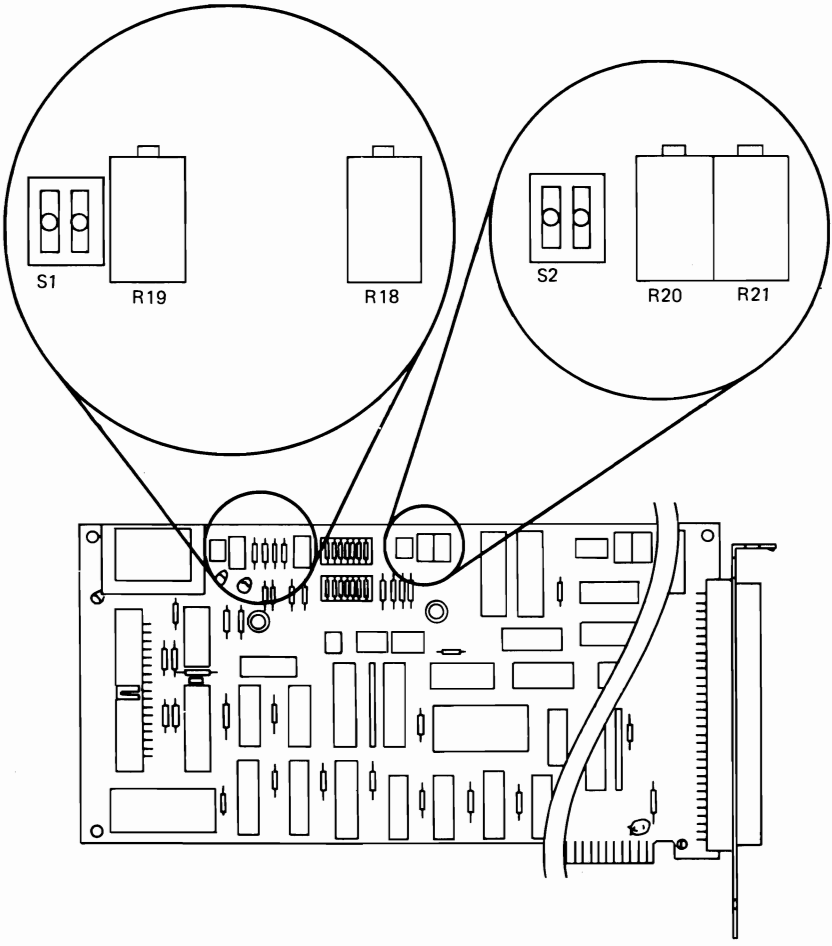
Analog Output Device Registers

AO Control Register — When the 'write D/A value' signal occurs, the digital-to-analog write value control circuitry either strobes D/A 0 or D/A 1, on the basis of the channel-select bit in the AO control register.

AO Data Register — When either AD7545 DAC receives a digital-to-analog write strobe, it latches a 12-bit digital value from the adapter's 16-bit data bus. Each DAC has data latches that are loaded when the AO data register address is written to. The AD7545 DAC then performs the digital-to-analog conversion, and an analog value is sent to the distribution panel connector by 'D/A 0 out' or 'D/A 1 out.'

Analog Output Potentiometers

Four potentiometers (R18, R19, R20, and R21) on the Data Acquisition Adapter control bipolar offset and gain for the analog output device. The following diagram shows the location of these potentiometers.



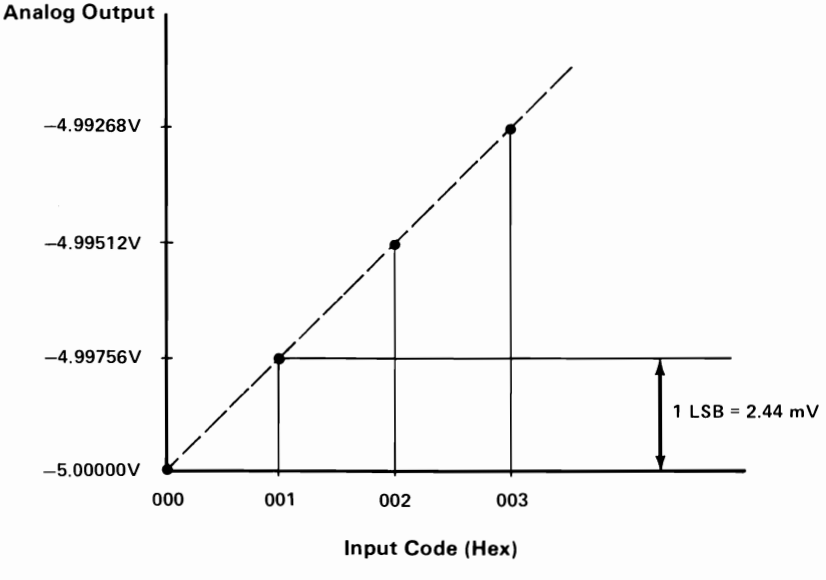
Bipolar Offset:

R18 controls bipolar offset for channel 0, and R20 controls it for channel 1. The value of the potentiometer is set so a negative full-scale voltage is provided on the analog output channel when the digital code 0000 0000 0000 is sent to the DAC for that channel. The potentiometer takes effect when a bipolar range is selected. When the unipolar range is selected, the DAC output is 0 volts.

The following table lists the output voltages for the digital code 0000 0000 0000 (000 hex).

Range	Output Voltage for 000 Hex Code
0 to +10 volts	0.00000 volts
-5 to +5 volts	-5.00000 volts
-10 to +10 volts	-10.00000 volts

The following shows the first few analog output voltages for the -5 to +5 volt range.



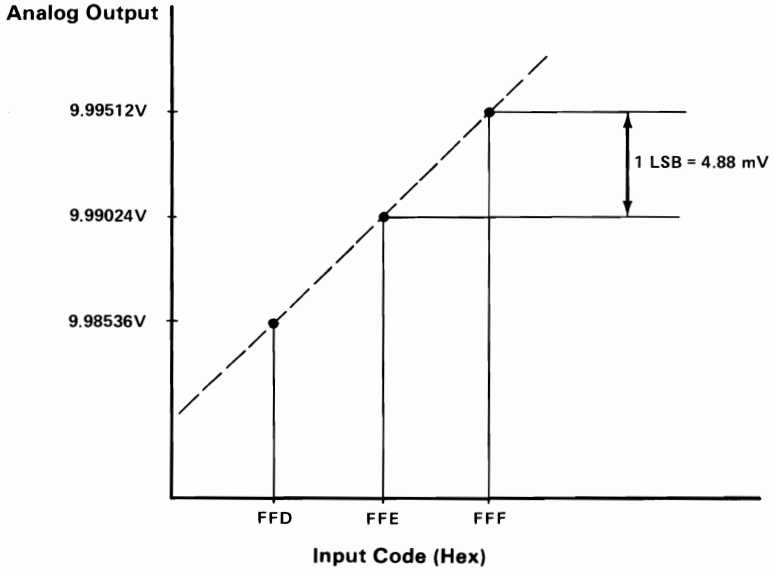
Gain:

R19 controls gain for channel 0, and R21 controls it for channel 1. The value of the potentiomenter is set so a positive full-scale −1 LSB voltage is provided on the analog output channel when the digital code 1111 1111 1111 is sent to the DAC for that channel.

The following table lists the output voltages for the digital code 1111 1111 1111 (FFF hex).

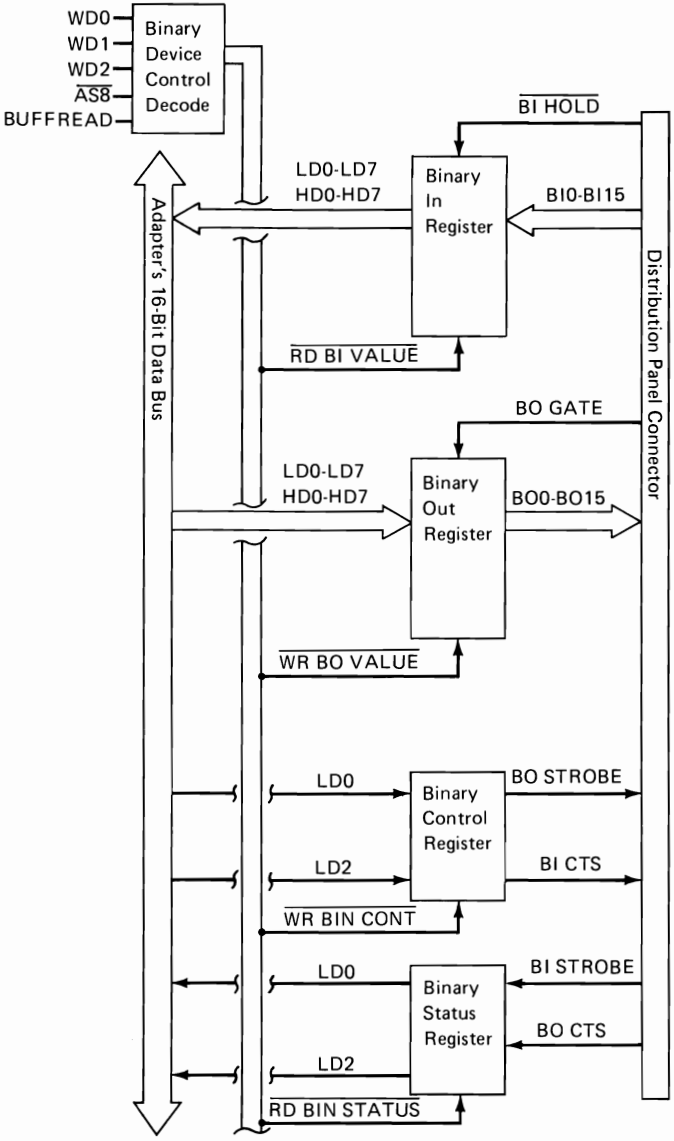
Range	Output Voltage for FFF Hex Code
0 to +10 volts	+9.99756 volts
-5 to +5 volts	+4.99756 volts
-10 to +10 volts	+9.99512 volts

The following shows the last few analog output voltages for the -10 to +10 volt range.



Binary I/O Device

Following is a block diagram of the binary I/O device.



The Data Acquisition Adapter's binary I/O device has the following features:

- A 16-bit binary output port (BO0 through BO15)
- A 16-bit binary input port (BI0 through BI15)
- Input and output handshaking over the 'strobe' and 'clear-to-send' lines
- Direct control using BO GATE ('binary out gate') and $\overline{\text{BI HOLD}}$ ('binary in hold').

Digital signals have only two voltage states: On (high, +3 volts) and Off (low, +0.2 volts). Digital signals in this range are called *TTL signals*, because they are the proper levels to be interpreted by the transistor-to-transistor logic circuitry. These signals have many uses in data acquisition and control applications. Among these are sensing the state of two-state devices and controlling devices that require two-state control signals.

Binary I/O Device Control

The use of the $\overline{AS8}$ strobe causes the binary I/O device to be accessed as device number 8.

The $\overline{AS8}$ strobe as an enable, the WD0 through WD2 word bits, and the BUFFREAD signal are used to decode which binary decode operation is to occur.

Following are the four decode operations:

$\overline{WR\ BIN\ CONT}$ — Write binary control: Controls the latching of the binary output strobe (BO STROBE) and the binary input clear-to-send (BI CTS) bits by the binary control register.

$\overline{RD\ BIN\ STATUS}$ — Read binary status: Controls the reading of the binary input strobe (BI STROBE) and the binary output clear to send (BO CTS) bits by the binary status register.

$\overline{WR\ BO\ VALUE}$ — Write binary value: Controls the writing of the binary output word (BO0 through BO15) to the binary output register.

$\overline{RD\ BI\ VALUE}$ — Read binary value: Controls the reading of the binary input word (BI0 through BI15) from the binary input data register.

Binary I/O Device Registers

Following is a description of the binary I/O device registers.

Binary Control Register

Contains the BO STROBE bit and the BI CTS bit. These bits do not physically cause or prevent binary I/O events from occurring. They are programming control bits.

Binary Status Register

Allows the status of BO CTS and BI STROBE bits to be monitored. These bits do not physically cause or prevent binary I/O events from occurring. They are programming status bits.

Binary Input Register

When $\overline{\text{BI HOLD}}$ is brought high (or if no connection is made), the binary input register is not latched and allows the current state of the binary input lines to be monitored by reading the binary input register. Grounding $\overline{\text{BI HOLD}}$ causes the binary input register to latch the current state of all binary input lines. If the grounding of the $\overline{\text{BI HOLD}}$ line is maintained, any later read will obtain the value that was present when the line was initially grounded.

Binary Output Register

Contains the binary output word (BO0 through BO15). Grounding the BO GATE signal places the binary output port in the tri-state condition (all points floating). The binary outputs are gated out when the BO GATE signal is brought high (or if no connection is made).

The Data Acquisition Adapter's binary I/O device consists of two subsystems that use low-power Schottky logic:

- Binary input
- Binary output

Binary Input Subsystem

Following is a description of the binary input subsystem.

Binary Input Port (BI0 through BI15)

All bits of the binary input port (BI0 through BI15) are pulled to their high state internally. This means that if nothing is connected to the binary input port, execution of a binary input function returns a value of 65535 (all bits set to 1).

The input port of the Data Acquisition Adapter's binary I/O device can be used to sense the state of up to 16 individual binary signals.

The binary input port also can be used for input of binary data words (16-bit) from another device.

Binary Input Hold

The entire binary input port may be latched at any time by pulling the $\overline{\text{BI HOLD}}$ signal low. These and all other data and communication lines are pulled high through internal resistors to +5 volts. No connections to them are necessary unless their features are to be used.

Binary Input Handshaking

Binary input samples can be synchronized with binary words generated by an external device. The external device must be able to send parallel binary data when it receives a signal from the Data Acquisition Adapter's binary I/O device. It also must be able to generate a TTL signal that indicates the data word is valid and should be sent by the Data Acquisition Adapter.

Binary Output Subsystem

Following is a description of the binary output subsystem.

Binary Output Port (BO0 through BO15)

This subsystem uses high-power, tri-state, bus-driving devices. Changes in the binary output word are carried out on a per-bit basis. Only those bits affected by a change in the output word are actually changed. All others remain the same.

The output port of the binary I/O device supplies 16 high/low signals under program control. As with the input port, these signals can be used individually or considered as a 16-bit data word.

Binary Out Gate

You may place the output port in tri-state by pulling the binary out gate (BO GATE) lines low. These and all other data, handshaking, and control lines are pulled high by internal resistors to +5 volts. No connections to them are necessary unless your application requires handshaking or control.

Binary Output Handshaking

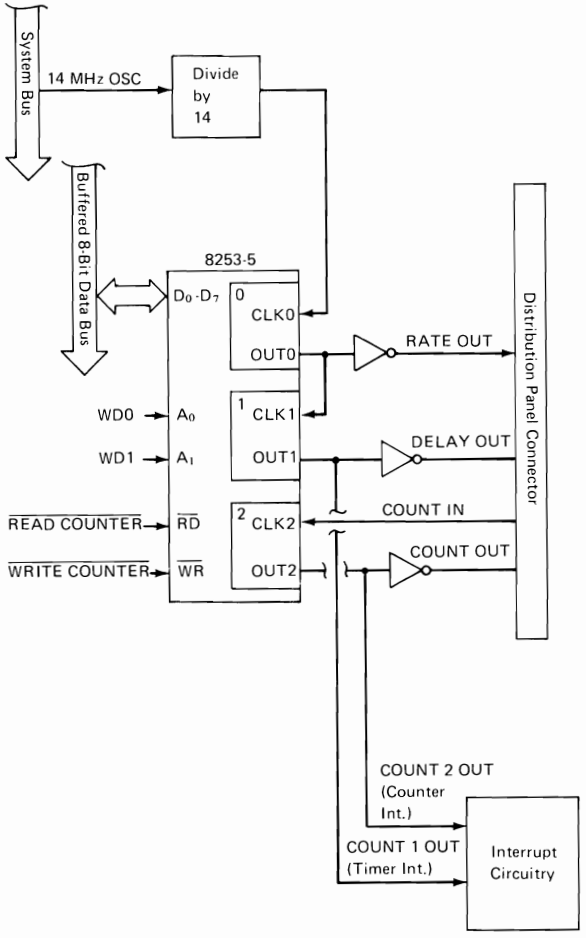
Because all communication lines are internally pulled up to their logical true state, you can use or not use binary output handshaking, depending on the requirements of your communication setup.

Binary output can be synchronized with the data input capabilities of the external device. The external device must be able to send a TTL signal to indicate it is ready for new data. It also must be able to accept parallel binary data when it recieves a signal from the Data Acquisition Adapter's binary I/O device indicating the data is available.

Timer/Counter Device

The timer/counter device is an 8253-5 Programmable Interval Timer. The timer/counter device provides three independent, down-counting, 16-bit counters. Each counter can be programmed to operate in one of four modes. In this implementation, Counters 0 and 1 are cascaded to provide a 32-bit timer. Counter 2 is not cascaded and provides an independent 16-bit timer/counter. These counters can be used to generate interrupts, provide pulses (or pulse trains) to the distribution panel connector (RATE OUT, DELAY OUT, and COUNT OUT), and count events (COUNT IN).

Following is a diagram of the timer/counter device.



Timer/Counter System Interface

Following is a description of how the Data Acquisition Adapter controls its timer/counter device.

BD0 - BD7 The Data Acquisition Adapter's buffered data bus lines are connected to data lines (D0 through D7) of the timer/counter device's internal data-bus buffer.

$\overline{\text{RD CNT}}$ Read counter: Connected to the RD pin of the timer/counter device. Used as a control signal when reading the values of the counters.

$\overline{\text{WR CNT}}$ Write counter: Connected to the WR pin of the timer/counter device. Used as a control signal when writing mode information and loading the counters.

WD0 and WD1 Connected to the A0 and A1 pins of the timer/counter device. They select which of the three counters to be operated on, and address the control register.

The following lists the resulting timer/counter device operations performed based on the values of the timer/counter device's address and control signals.

Note: The CS pin of the timer/counter device is tied low.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	Description
0	1	0	0	0	Load Counter 0
0	1	0	0	1	Load Counter 1
0	1	0	1	0	Load Counter 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

32-Bit Timer

Following is a description of the output of the 32-bit timer (Counters 0 and 1), and how it is clocked.

First Stage (Counter 0)

CLK 0	A 1.023-MHz signal (50% duty cycle) from the system bus' 14-MHz OSC and divide-by-14 circuitry.
OUT 0	Output of Counter 0.
RATE OUT	Inverted state of OUT 0 that is brought to the distribution panel connector.

Second Stage (Counter 1)

CLK 1	The Counter-1 clock. The output of Counter 0 (OUT 0) is cascaded into the counter of clock 1.
OUT 1	Output of Counter 1. Provides the 'count 1 out' signal that is used by the interrupt circuitry.
DELAY OUT	Inverted state of OUT 1 that is brought to the distribution panel connector.

16-Bit Timer/Counter

Following is a description of the output of the 16-bit timer/counter (Counter 2), and how it is clocked.

CLK 2	The Counter-2 clock.
COUNT IN	Clocks Counter 2.
OUT 2	Output of Counter 2. Provides the 'count 2 out' signal used by the interrupt circuitry.
COUNT OUT	Inverted state of OUT 2 that is brought to the distribution panel connector.

Counter Modes

The following counter modes apply to Counters 0 through 2.

> **Note:** "Output" in the following timing diagrams refers to the OUT 0, OUT 1, and OUT 2 pins of the timer/counter device. Counter outputs, RATE OUT, DELAY OUT, and COUNT OUT, on the distribution panel connector are the inverted state of OUT 0, OUT 1, and OUT 2.

Mode 0: Interrupt on Terminal Count

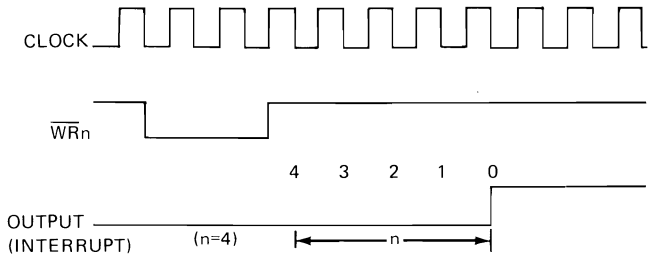
Initially, the output is low after the mode-set operation. After the count is loaded into the selected count register, the output remains low, and the counter counts. When terminal count is reached, the output goes high and remains high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrease after terminal count is reached.

Rewriting a counter register during counting results in the following:

- A Write to the first byte stops the current counting.
- A Write to the second byte starts the new count.

Following is the timing diagram for mode 0.

Mode 0: Interrupt on Terminal Count



Mode 1: Programmable One-Shot

This mode is not used because the timer/counter device's gate pins (GATE 0 through GATE 2) are tied high.

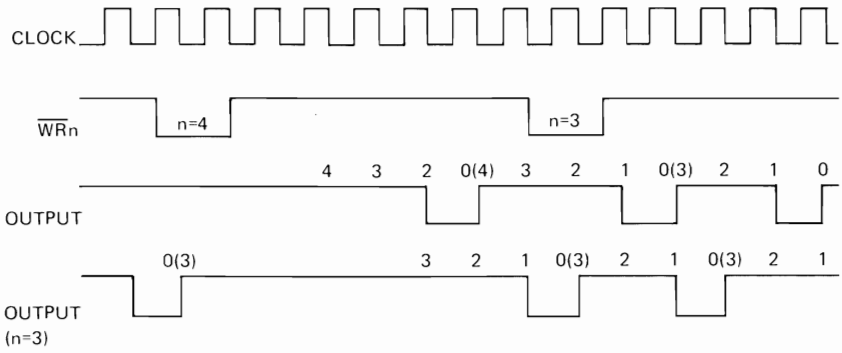
Mode 2: Rate Generator

Divide-by-N counter. The output is low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses, the present period is not affected, but the next period reflects the new value.

When the mode is set, the output remains high until the count register is loaded. The output can then also be synchronized by programming.

Following is the timing diagram for mode 2.

Mode 2: Rate Generator



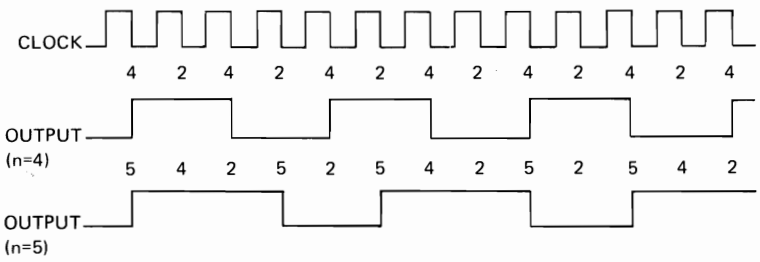
Mode 3: Square-Wave Rate Generator

This mode is similar to mode 2, except the output remains high until half the count is complete (for even numbers), then goes low for the other half. This is accomplished by decrementing the counter by 2 on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output changes, and the counter is reloaded with the full count; the complete process then repeats.

If the count is odd and the output high, the first clock pulse after the count is loaded, decreases the count by 1. Subsequent clock pulses decrease the clock by 2. After time-out, the output goes low and the full count is reloaded. The first clock pulse after the reload, decreases the counter by 3. Subsequent clock pulses decrease the count by 2 until time-out. Then the complete process repeats. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Following is the timing diagram for mode 3.

Mode 3: Square Wave Generator



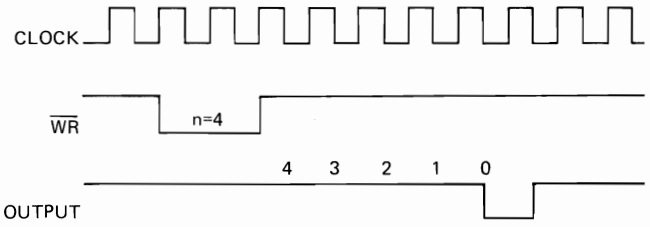
Mode 4: Software-Triggered Strobe

After the mode is set, the output is high. When the count is loaded, the counter begins counting. When the counter reaches terminal count, the output goes low for one input clock period, then goes high again.

If the count register is reloaded during counting, the new count is loaded on the next CLK pulse.

Following is the timing diagram for mode 4.

Mode 4: Software Triggered Strobe

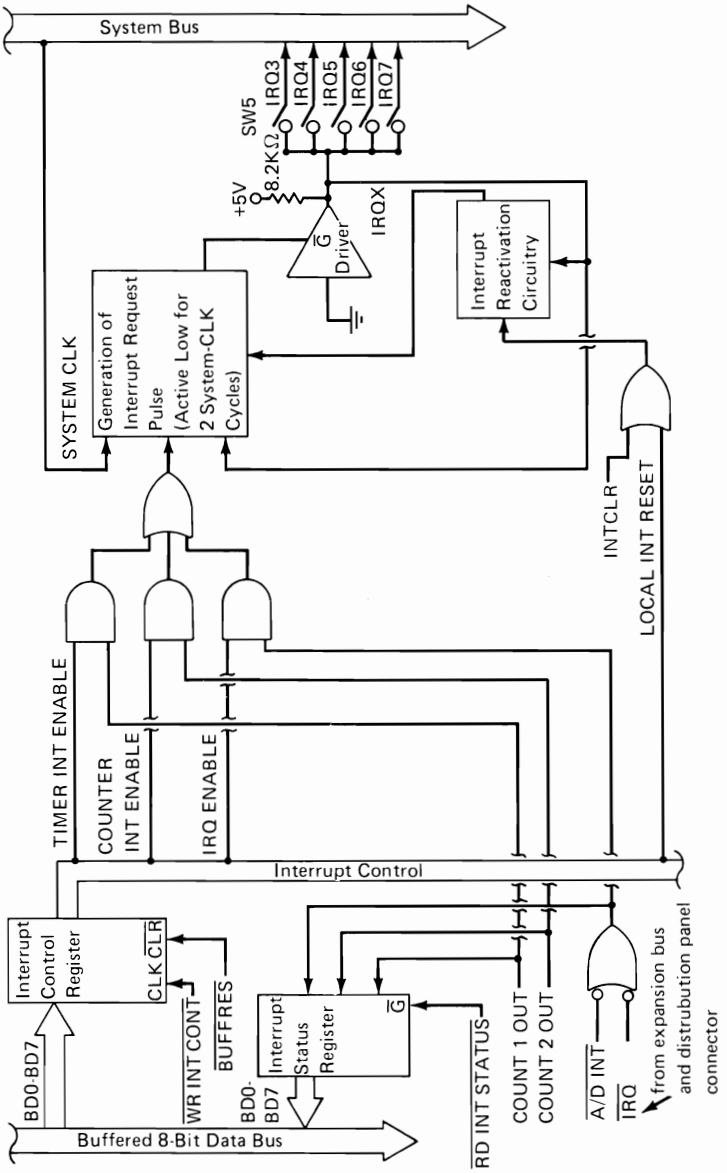


Mode 5: Hardware-Triggered Strobe

This mode is not used because the pins for gates 0 through 2 are tied high.

Interrupt Circuitry

The following is a block diagram of the interrupt circuitry.



The Data Acquisition Adapter can generate an interrupt from the following individually maskable sources:

- 32-bit timer (cascaded 16-bit Counters 0 and 1 of the timer/counter device)
- 16-bit externally-clocked timer/counter (Counter 2 of the timer/counter device)
- ADC 'end of conversion' signal
- IRQ external interrupt (on the distribution panel connector and the expansion bus).

Interrupts generated by the Data Acquisition Adapter can be set to an interrupt level in the range of IRQ3 through IRQ7. The interrupt level is set with the switches of S5 on the adapter and must be set before adapter installation. IRQ7 is recommended.

Interrupt Control Register

Following is a description of the bits of the interrupt control register.

Bit 0 TINT ENABLE: Enables 32-bit timer interrupts (Counters 0 and 1).

Bit 1 CINT ENABLE: Enables 16-bit timer/counter interrupts (Counter 2).

Bit 2 IRQ ENABLE: Enables the $\overline{\text{IRQ}}$ (external interrupt) line and analog-to-digital end-of-conversion interrupts as sources of interrupts.

Bit 3 Reserved for reading status.

Bit 4 - 6 Not used.

Bit 7 LINT RESET: Performs the local-reset function.

Note: Power-on-reset ($\overline{\text{BUFFRES}}$) resets the interrupt control register (clearing all bits and disabling interrupts).

Interrupt Status Register

Following is a description of the bits of the interrupt status register.

Bits 0 - 3 Provided for reading the status of the corresponding interrupt-enable bits listed under "Interrupt Control Register". Bit 3 is not currently used.

Bit 4 TINT STAT: The timer interrupt status (COUNT 1 OUT), which is the state of the output of the second chained timer stage (Counter 1 of the timer/counter device).

Bit 5 CINT STAT: The counter interrupt status (COUNT 2 OUT), which is the state of the output of the 16-bit timer/counter (Counter 2).

Bit 6 IRQ STAT: The $\overline{\text{IRQ}}$ (external-interrupt) status. The on-board 'A/D interrupt' signal is logically ORed into the $\overline{\text{IRQ}}$ (external-interrupt) function.

Bit 7 Read back as a 0.

Interrupt Request Pulse

The corresponding three interrupt-enable and three interrupt-status lines are logically ANDed. Any combination of the three interrupt sources may be enabled. The enabled interrupts are logically ORed to generate the adapter-interrupt trigger signal. This signal causes the generation of an 'interrupt request out' pulse by enabling a tri-state driver to be active low for two cycles of the system clock. The output of this driver is connected to the desired system interrupt level (IRQ3 through IRQ7) by switch S5. When not active low, the tri-state driver is floating and allows other adapters to share the interrupt line.

Interrupt Reactivation

When the shared-interrupt line pulses low, regardless of whether the Data Acquisition Adapter or another interrupt-sharing adapter was the source, the interrupt-reactivation circuitry prevents the Data Acquisition Adapter from generating interrupts. Thus, a single interrupt causes deactivation of additional interrupts. Additional interrupts are reactivated by either the 'local reset' signal (only one Data Acquisition Adapter reactivated) or the INTCLR signal (all interrupt-sharing adapters reactivated). A logical OR of the 'local reset' or INTCLR shared-interrupt reactivation signals starts the interrupt-reactivation circuitry.

Following is a description of the two shared-interrupt reactivation signals.

Local Interrupt Reset

The local-interrupt-reset bit in the interrupt control register controls the reactivation of only one Data Acquisition Adapter. The particular adapter is singled out by the adapter-number bits (A10 and A11) in the adapter's I/O address space.

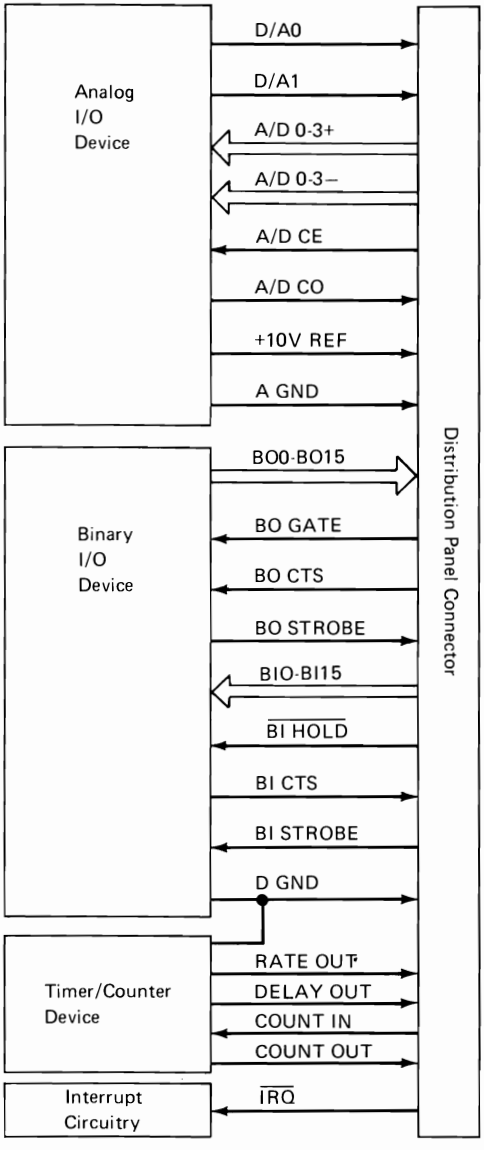
Global Interrupt Reset

A global-interrupt reset also can be performed. This resets the interrupt circuitry of all adapters sharing a particular interrupt level. The only requirement is that the adapters support interrupt sharing. The Data Acquisition Adapter does support interrupt sharing.

To perform a shared-interrupt global reset, an I/O Write to an address hex 02Fx (02F3 through 02F7) is performed for a particular interrupt level (IRQ3 through IRQ7). Thus, to reset all adapters sharing interrupt IRQ7, an I/O Write to hex 02F7 is performed. The output value is not important.

Distribution Panel Connector

Following is a block diagram of the signals of the distribution panel connector, J4.



Distribution Panel Connector Signals

The following is a description of how the distribution panel connector, J4, provides access to the interrupt circuitry, and the analog I/O, binary I/O, and timer/counter devices.

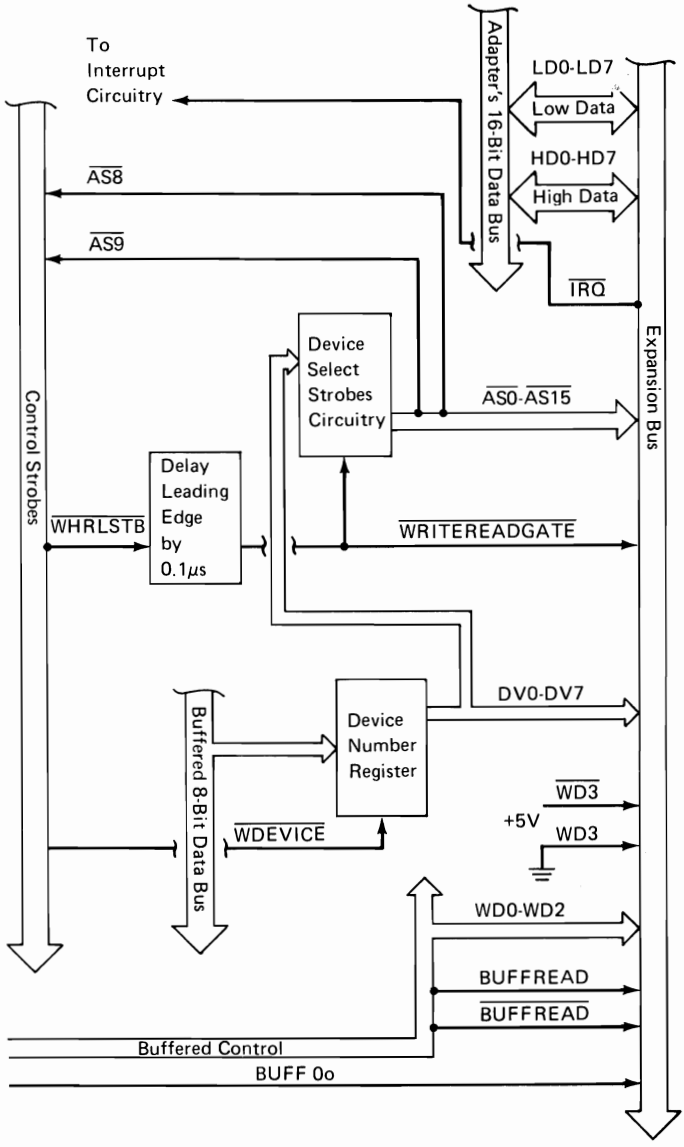
D/A 0, D/A 1	DAC outputs.
EXT +10 V REF	10-volt reference output.
A GND	Analog ground: The system ground reference for the analog devices in the system.
A/D 0- to A/D 3-	Channels 0 through 3 ADC inputs (low).
A/D 0+ to A/D 3+	Channels 0 through 3 ADC inputs (high).
D GND	Digital ground: The system ground reference for the digital devices in the system.
A/D CE	'Convert enable' input for the ADC. When high, enables conversion.
A/D CO	'Convert out' indicator for the ADC. When high, indicates a conversion was requested. Returns to low when the conversion is complete.

$\overline{\text{BI HOLD}}$	Binary-input hold: Latch control for the binary input port. When low, the binary input device latches the state of all input lines.
BI STROBE	(Input) Binary input strobe: When high, indicates the binary input data is available.
BI0 - BI15	Binary input port, bits 0 through 15.
BO0 - BO15	Binary output port, bits 0 through 15.
BO GATE	(Input) Binary output gate: Tri-state enable for the binary output port. When low, the binary outputs (BO0 through BO15) are floating.
BO STROBE	(Output) Binary output strobe: When high, indicates that new data was sent.
BO CTS	(Input) Binary output clear-to-send: When high, permits new binary-output port data to be sent.
BI CTS	(Output) Binary input clear-to-send: When high, indicates the binary input data is being requested.

$\overline{\text{IRQ}}$	(Input) External-device, interrupt-request: Active low.
RATE OUT	Output from the first stage of the 32-bit timer (Counter 0). The 'rate out' signal is the inverse of the timer/counter device output.
DELAY OUT	Output from the second stage of the 32-bit timer (Counter 1). The 'delay out' signal is the inverse of the timer/counter device output.
COUNT OUT	Output from the 16-bit counter device (Counter 2). The 'count out' signal is the inverse of the timer/counter device output.
COUNT IN	Input to the 16-bit counter device (Counter 2).

Expansion Bus

Following is a block diagram showing device selection signals, control signals, and data bus lines which make up the expansion bus.



August 15, 1984

The expansion bus is an expansion interface for data acquisition and control adapters. The bus consists of two 34-pin transition connectors, J1 and J2, on the Data Acquisition Adapter.

All drivers on the bus are intended to be low-power Schottky (LS) TTL bus drivers or equivalent devices. Such devices can drive below 0.4 volts at 12 milliamperes load current, and above 2.4 volts at 2.6 milliamperes.

All receivers on the bus are intended to be no more than two LS TTL loads for each external device on any bus line. Such devices will present a load current of no more than 0.8 milliamperes sourcing at 0.4 volts, and no more than 40 microamperes sinking at 2.4 volts. A single LS TTL load for each external device on any bus line is preferred.

Drivers on the bidirectional data lines must be tri-state devices enabled only during the appropriate strobes.

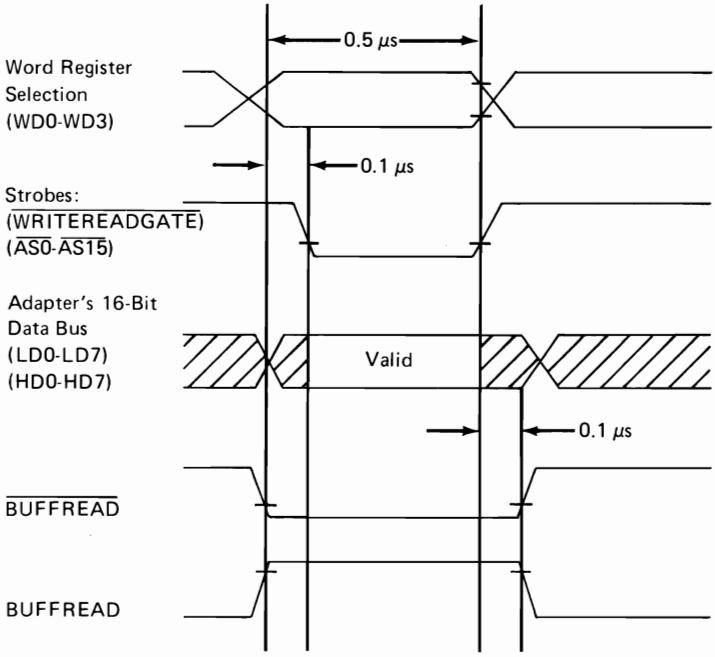
Expansion Bus Signals

Following is a description of the signals on the expansion bus.

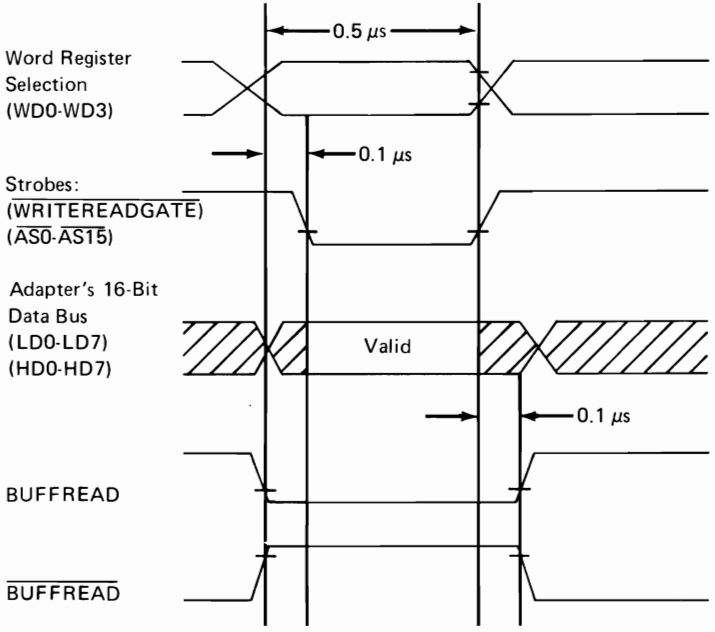
BUFF 0_0	(Output) OSC signal divided by 14 (1.023 MHz).
$\overline{\text{WRITEREADGATE}}$	(Output) Active low strobe for all devices. $\overline{\text{AS16}}$ through $\overline{\text{AS255}}$ strobes can be created by decoding DV0 through DV7 and using the signal, $\overline{\text{WRITEREADGATE}}$.
BUFFREAD	(Output) When high, indicates a read is occurring. When low, indicates a write is occurring.
$\overline{\text{BUFFREAD}}$	(Output) Inverse of BUFFREAD.
$\overline{\text{BUFFRES}}$	(Output) inverse of RESET DRV. Performs system reset and initialization.
$\overline{\text{IRQ}}$	(Input) External, interrupt request. Active low.
$\overline{\text{AS0}}$ to $\overline{\text{AS15}}$	(Outputs) Active low strobes for devices 0 through 15. Must be low for 0.4 microseconds.

$\overline{\text{WD3}}$	Word number bit 3, fixed high.
WD3	Word number bit 3, grounded.
HA4 - HA7	Reserved expansion signals; grounded.
DV0 - DV7	(Output) Device-number bits. Select one of 256 possible devices.
LD0 - LD7	(Inputs/Outputs) Low byte of the adapter's 16-bit data bus.
HD0 - HD7	(Inputs/Outputs) High byte of the adapter's 16-bit data bus.
WD0 - WD2	Word number bits 0 through 2 (system-bus address lines A12 through A14 are buffered and renamed WD0 through WD2).

Following is a diagram of the expansion bus read timing.



Following is a diagram of the expansion bus write timing.



Programming Considerations

This section describes the programming considerations for the Data Acquisition Adapter.

Address Decoding

The following table shows address decoding.

A15 A14 A13 A12	A11 A10	A9 A8 A7 A6 A5 A4 A3 A2 A1	A0
Register Select	Card Select	1 0 1 1 1 0 0 0 1	Byte Select

- Register Select selects one of 16 word registers (0 through 15). Only registers 0 through 13 are used.
- Card Select selects the adapter number (0 through 3).
- A1 through A9 are a fixed pattern to select Data Acquisition Adapters.
- A0 selects the high or low byte of a 16-bit word register.

The base addresses of the Data Acquisition adapters are:

Adapter Number	Base Address (Hex)
0	02E2
1	06E2
2	0AE2
3	0EE2

Registers

Each Data Acquisition Adapter has 16 (two-byte) word registers through which all access to the Data Acquisition Adapter is made. The registers allow access to the Data Acquisition Adapter's on-board and expansion data-acquisition and control devices, the adapter's interrupt registers and device number register, and the timer/counter device registers.

The following table shows the Data Acquisition Adapter's registers.

Register	Name	Function
0 1 2 3 4 5 6 7	Device Register 0 Device Register 1 Device Register 2 Device Register 3 Device Register 4 Device Register 5 Device Register 6 Device Register 7	Write values to, and read values from, the on-board and external devices
8	Timer/Counter 0 Register	Read/load Counter 0
9	Timer/Counter 1 Register	Read/load Counter 1
10	Timer/Counter 2 Register	Read/load Counter 2
11	Timer/counter Control Register	Controls the operation of Counters 0 through 2.
12	Device Number	Selects device
13	Interrupt Registers	Interrupt control and status
14		Not used
15		Not used

Device Registers

Eight register addresses have been reserved for reading and writing the registers on the on-board and external devices. The device is selected using the device-number register. These registers may then be used for access to the registers of that device. These registers are both read and write registers, and often two different functions will be decoded for the read and write.

Analog Input Device Registers

The on-board analog input (AI) device, accessed as device number 9, has four channels. External AI devices can be added to the expansion interface. These external AI devices have up to 256 channels, use ADCs with up to 16 bits of resolution, and are accessed with a different device number, but with the same register format as the on-board AI device.

The AI device has the following registers.

Register	Read/Write	Name	Function
0	Write	AI Control	Sets up and controls the register.
0	Read	AI Status	Returns status of the hardware.
2	Read	AI Data	Returns current analog value.

Following is a description of the bits of the AI control register.

Bit	Name	Function
0	Convert Start	Setting this bit starts an analog-to-digital conversion.
1	Short Cycle	Reserved for enabling a short cycle conversion.
2	EOCINT Enable	End-of-conversion interrupt enable. When set, an end-of-conversion (conversion complete) will generate an interrupt.
3-7		Not used
8-15	Channel	Channels 0 through 255. On-board AI device uses only channels 0 through 3.

Following is a description of the bits of the AI status register.

Bit	Name	Function
0	Busy State	When set, indicates that the ADC is in the process of doing a conversion and data is not yet valid.
1	Int State	When set, indicates that a conversion has ended (not busy and interrupting state). If the EOCINT enable bit is set (enabled), an interrupt is generated.
2	EOCINT Enable	Read back of state of EOCINT enable bit in AI control register.
3 - 15		Not used

Following is a description of the bits of the AI data register.

Bit	Name	Function
0-15	Data	Contains the data value from the last conversion. Valid only if the busy bit in the AI status register is cleared. Bits 0 through 11 will contain data from the 12-bit ADC. Bits 12 through 15 will all be zeros.

AI Device Access Strategy

The following outlines the access strategy for the AI device. Note that because channel selection takes a while, routines that repeatedly access a single channel would want to select the channel only once before data acquisition.

Polling Method

To use the polling method, do the following:

1. Set the device number in the device-number register to 9.
2. Set the channel and simultaneously disable conversion by setting the convert start bit to 0.
3. Wait for the channel multiplexer to settle (approximately 20 microseconds).
4. Request a conversion by setting the convert start bit to 1 and set the same channel.
5. Wait for the busy stat bit to equal 0.
6. Enable reading of the ADC's data by setting the convert start bit to 0, and set the same channel.
7. Read the data value.

Interruption Method

To use the interruption method, do the following:

1. Set the device number in the device-number register to 9.

2. Set the channel and simultaneously disable conversion by setting the convert start bit to 0.

3. Wait for the channel multiplexer to settle (approximately 20 microseconds).

4. Request a conversion by setting the convert start bit to 1, and set the same channel.

5. Set the EOCINT enable bit to 1 to enable an end-of-conversion interrupt.

6. After servicing the interrupt, set the EOCINT enable bit to 0 to disable AI interrupts.

Analog Output Device

The analog output (AO) device has two channels, uses 12-bit DACs, and is accessed as device number 9.

External AO devices can be added to the expansion interface. These devices have up to 256 channels, use DACs with up to 16-bit resolution, and are accessed with a different device number, but use the same register format as the analog output device.

The AO device has the following registers.

Register	Read/Write	Name	Function
1	Write	AO Control	Sets up and controls the register.
3	Write	AO Data	Output value.

Following is a description of the bits of the AO control register.

Bit	Name	Function
0-7		Not used
8-15	Channel	Selects channel 0 through 255. On-board AO device uses channels 0 and 1.

Following is a description of the bits of the AO data register.

Bit	Name	Function
0-15	Data	The value to be provided to the selected channel. Sets bits 0 through 11 with data for the 12-bit DACs, and bits 12 through 15 with zeros.

AO Device Access Strategy

To use the AO device access strategy, do the following:

1. Set the device number to 9 in the device-number register.
2. Set the channel in the AO control register.
3. Write the data value to the AO data register.

Binary Input/Output Device

This on-board device, which is accessed as device number 8, is a parallel binary (TTL) I/O device. It has one 16-bit output port, one 16-bit input port, and support for handshaking lines.

Binary I/O expansion devices can be attached to the expansion interface. These devices are accessed with a different device number, but use the same register format as the binary I/O device.

The binary I/O device has the following registers.

Reg.	Read/Write	Name	Function
0	Read	Binary Status	The current state of the handshaking input lines.
0	Write	Binary Control	Controls the state of the handshaking output lines.
2	Read	Binary Input	Data register for binary input port.
2	Write	Binary Output	Data register for binary output port.

Following is a description of the bits of the binary status register.

Bit	Name	Function
0	BI Strobe	Indicates the state of the binary input port's 'BI strobe' input handshaking line.
1		Reserved
2	BO CTS	Indicates the state of the binary output port's 'clear to send' (BO CTS) input handshaking line.
3		Reserved
4-15		Not used

Following is a description of the bits of the binary control register.

Bit	Name	Function
0	BO Strobe	This bit sets and clears the binary output port's 'BO strobe' output handshaking line.
1		Reserved
2	BI CTS	This bit sets and clears the binary input port's 'clear to send' (BI CTS) output handshaking line.
3-4		Reserved
5-15		Not used

Following is a description of the bits of the binary input register.

Bit	Name	Function
0-15	Data	The current value at the binary input port can be read from this register. The value contained is not latched (unless 'BI hold' was used).

Following is a description of the bits of the binary output register.

Bit	Name	Function
0-15	Data	The value to be placed on the binary output port is written here. Data lines of the port are affected as soon as the register is written.

Binary Input Access Strategies

To use binary input with handshaking, do the following:

1. Set the device number to 8 in the device-number register.
2. Set BI CTS high in the binary control register.

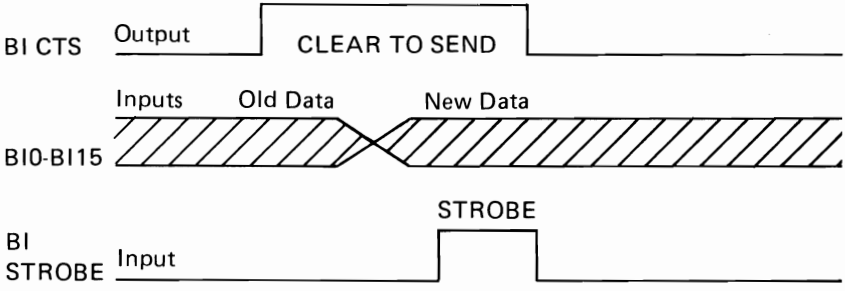
   The external device puts new data on the binary input lines (BI0 through BI15) at the distribution panel connector.

   The data on the input lines must remain valid until BI CTS is lowered.

   The external device sets 'BI strobe' high.
3. Read data from the binary input register.
4. Reset BI CTS in the binary control register.

   The external device lowers 'BI strobe.'

Following is a diagram showing binary input with handshaking.



To use binary input without handshaking, do the following:

1. Set the device number to 8 in the device-number register.
2. Read the data value from the binary input register.

Binary Output Access Strategies

To use binary output with handshaking, do the following:

1. Set the device number to 8 in the device-number register.

   The external device lets BO CTS go high on the distribution panel connector. This is detected by reading the binary status register's BO CTS bit.

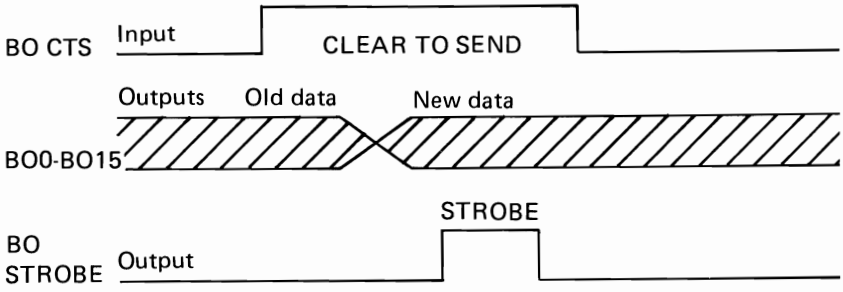
2. Write the new data value to the binary output register.

3. Set the binary control register's 'BO strobe' bit.

4. Reset the 'BO strobe' bit in the binary control register.

   The external device releases BO CTS.

The following diagram shows binary output with handshaking.



To use binary output without handshaking, do the following:

1. Set the device number to 8 in the device-number register.

2. Write the data value to the binary output register.

Timer/Counter Device Registers

This section describes the timer/counter's control register, loading of the counters, its write operations, programming format, and read operations.

The timer/counter device has the following registers.

Reg.	Read/Write	Name	Function
8	Read/Write	Timer/Counter 0 Register	Read/load Counter 0
9	Read/Write	Timer/Counter 1 Register	Read/load Counter 1
10	Read/Write	Timer/Counter 2 Register	Read/load Counter 2
11	Write	Timer/counter Control Register	Controls the operation of Counters 0 through 2.

Control Register

The timer/counter's control register controls the operating mode of each counter, selection of binary or binary coded decimal (BCD) counting, and how each counter register is loaded. The control register can only be written to; no read operation of its contents is available.

The table on the following page shows control-word information for the timer/counter's control register.

Control Word Format

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definitions of Control

SC - Select Counter:

SC1	SC0	Description
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL - Read/Load:

RL1	RL0	Description
0	0	Counter latching operation
1	0	Read/load most significant byte (MSB) only.
0	1	Read/load least significant byte (LSB) only.
1	1	Read/load LSB first, then the MSB.

M - MODE:

M2	M1	M0	Description
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD - Binary Coded Decimal:

0	Binary counter 16-bits
1	BCD counter (4 decades)

Counter Loading

A count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits) and followed by a rising edge and a falling edge of the clock. Any reading of the counter before that falling clock edge may yield invalid data.

Timer/Counter Write Operations

Each counter of the timer/counter must be programmed with the mode and quantity desired. The programmer must write to the timer/counter's control register, a control word containing mode information and the programmed number of count register bytes (1 or 2) before actually using the selected counter.

Writing the control word can be in any sequence of counter selection (Counter 0 does not have to be first or Counter 2 last). Each counter's control word has a separate address so that its loading is completely independent of sequence. However, the loading of the count register with the actual count value must be done in the exact sequence programmed in the control word (RL0 and RL1). This loading, like that of the control word, is still sequence-independent, but when a selected count register is loaded, it must be done with the number of bytes programmed in the control word. The one or two bytes, loaded in the count register, do not have to immediately follow the associated control word, they can be programmed at any time after the control word is loaded, as long as the correct number of bytes is loaded in order.

All counters are *down counters*. Thus, the value loaded into the count register will actually be decreased. Loading all zeroes into a count register results in the maximum count (2 to the 16th for binary, or 10 to the 4th for BCD). In mode 0, the new count does not restart until loading is complete. The count register will accept one or two bytes, depending on how the mode control words (RL0 and RL1) are programmed. Then the restart operation proceeds.

Timer/Counter Programming Format

The programming format shown below is a simple example of timer/counter loading and does not imply that it is the only format that can be used.

Programming Format:

MODE	Control Word Counter n
LSB	Count Register Byte Counter n
MSB	Count Register Byte Counter n

Alternate Programming Format:

Number	Byte	Description	Reg.
1	MODE	Control Word Counter 0	8
2	MODE	Control Word Counter 1	8
3	MODE	Control Word Counter 2	8
4	LSB	Count Register Byte Counter 1	9
5	MSB	Count Register Byte Counter 1	9
6	LSB	Count Register Byte Counter 2	10
7	MSB	Count Register Byte Counter 2	10
8	LSB	Count Register Byte Counter 0	11
9	MSB	Count Register Byte Counter 0	11

Timer/Counter Read Operations

In most counter applications, it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common applications that use this function. The timer/counter has logic that allows the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

The programmer can use two methods to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. The only requirement of this method is that the actual operation of the selected counter must be inhibited by external logic that inhibits the clock input (only valid for Counter 2, because its 'clock in' signal is brought to the distribution panel connector). This requirement ensures a stable count reading.

The contents of the selected counter are as follows:

- The first I/O Read contains the least-significant byte.
- The second I/O Read contains the most-significant byte.

Because of the timer/counter's internal logic, the entire reading procedure must be finished. If two bytes are programmed to be read, then the two bytes must be read before any loading-write (WR) commands can be sent to the same counter.

The following chart has information about the read operation.

Reg.	Description
8	Read Counter 0
9	Read Counter 1
10	Read Counter 2

The second method of reading the value of the counters involves reading while counting.

To allow the programmer to read the contents of any counter without affecting the counting operation, special internal logic of the timer/counter can be accessed with simple write commands to the mode register. When the programmer wishes to read the contents of a selected counter, he loads the mode register with a special code that latches the present count value into a storage register so that its contents have an accurate, stable quantity. The programmer then issues a normal Read command to the selected counter, and the contents of the latched register are available.

The second method of reading the counters has the same limitation as the first method described. That is, the entire read operation must be finished as programmed. The Read command has no effect on the counter's mode.

The following table shows the control word used for latching count. This control word is written to the timer/counter's control register.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

Note:

SC1, SC0 - specify counter to be latched
D5, D4 - 00 designates counter latching operation
X - don't care

Device Number Register

The device-number register selects the device to be accessed. Only the low-order byte should be written.

The on-board devices are:

- Analog I/O device (device number 9)
- Binary I/O device (device number 8)

The following table describes the bits of the device-number register.

Bit	Name	Function
0-7	Device Number	Selects which device to address (0-255)
8-15		Not used

Interrupt Registers

Two registers are decoded for register 13, the interrupt control register and the interrupt status register. The interrupt control register may be written to for setting up the Data Acquisition Adapter for various interrupts. The interrupt status register may be read for information about the Data Acquisition Adapter's current interrupt status.

The following is a description of the bits of the interrupt control register.

Bit	Name	Function
0	TINT Enable	Enables the timer-generated interrupts.
1	CINT Enable	Enables counter-generated interrupts.
2	IRQ Enable	Enables the external IRQ line to generate an interrupt. It also enables AI end-of-conversion interrupts. To enable EOC interrupt, both this bit and the EOCINT enable bit in the AI control register must be set.
3		Reserved. Must be cleared.
4-6		Not used. Must be cleared.
7	LINT Reset	Local Interrupt Reset; re-enables the interrupt circuitry of the addressed Data Acquisition Adapter.

The following is a description of the bits of the interrupt status register.

Note: The bits of the interrupt status register contain the current state of the devices that generate an interrupt. They are not latched, and they are not reset by reading them.

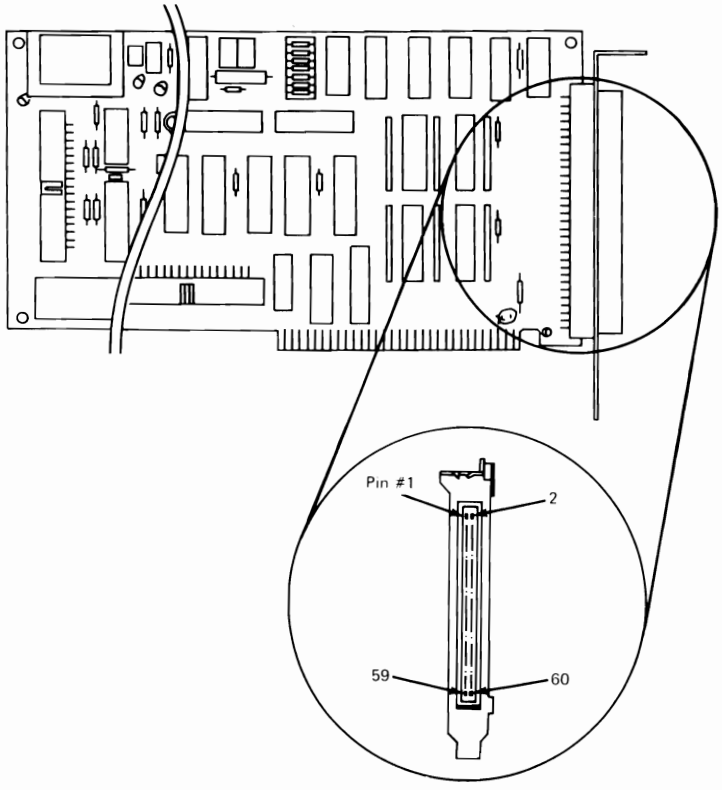
Bit	Name	Function
0 - 3	TINT Enable CINT Enable IRQ Enable	Read back of the current state of bits 0 through 3 in the interrupt control register.
4	TINT STAT	Timer Interrupt Status; if this bit is set, a timer-generated interrupt has occurred.
5	CINT STAT	Counter Interrupt Status; if this bit is set, a counter-generated interrupt has occurred.
6	IRQ STAT	$\overline{\text{IRQ}}$ Status; if this bit is set, the $\overline{\text{IRQ}}$ line generated an interrupt.
7		Reserved

Interface

Following is information about the Data Acquisition Adapter's connectors, J4 (distribution panel), and J1 and J2 (expansion bus).

Distribution Panel Connector

The following shows the location of the distribution panel connector (J4).



The following shows the pins of the distribution panel connector and their respective signals.

	Signal Name/Description	Pin	
	D/A 1	1	
	D/A 0	2	
	+10V REF	3	
	A GND	4	
	A/D 0-	5	
	A/D 0+	6	
	A/D 1-	7	
	A/D 1+	8	
	A/D 2-	9	
	A/D 2+	10	
	A/D 3-	11	Data
External	A/D 3+	12	Acquisition
Device	A GND	13	Adapter
	A/D CE	14	
	D GND	15	
	A/D CO	16	
	BI 8	17	
	BO 8	18	
	BI 9	19	
	BO 9	20	
	BI 10	21	
	BO 10	22	
	BI 11	23	
	BO 11	24	
	BI 12	25	
	BO 12	26	
	BI 13	27	
	BO 13	28	
	BI 14	29	
	BO 14	30	

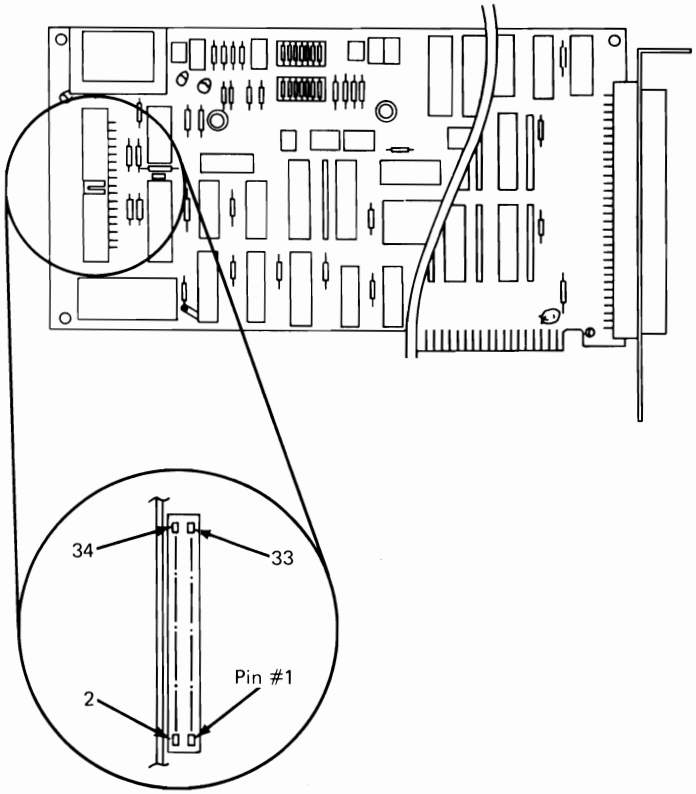
	Signal Name/Description	Pin	
	BI 15	31	
	BO 15	32	
	$\overline{\text{BI HOLD}}$	33	
	BO GATE	34	
	BI 0	35	
	BO 0	36	
	BI 1	37	
	BO 1	38	
	BI 2	39	
	BO 2	40	
	BI 3	41	Data
External	BO 3	42	Acquisition
Device	BI 4	43	Adapter
	BO 4	44	
	BI 5	45	
	BO 5	46	
	BI 6	47	
	BO 6	48	
	BI 7	49	
	BO 7	50	
	RATE OUT	51	
	DELAY OUT	52	
	BI STROBE	53	
	BO STROBE	54	
	BO CTS	55	
	BI CTS	56	
	$\overline{\text{IRQ}}$	57	
	COUNT OUT	58	
	COUNT IN	59	
	D GND	60	

Expansion Bus Connectors

Following is information about the expansion bus connectors (J1 and J2).

Expansion Bus Connector J1

The following shows the location of the expansion bus connector, J1.

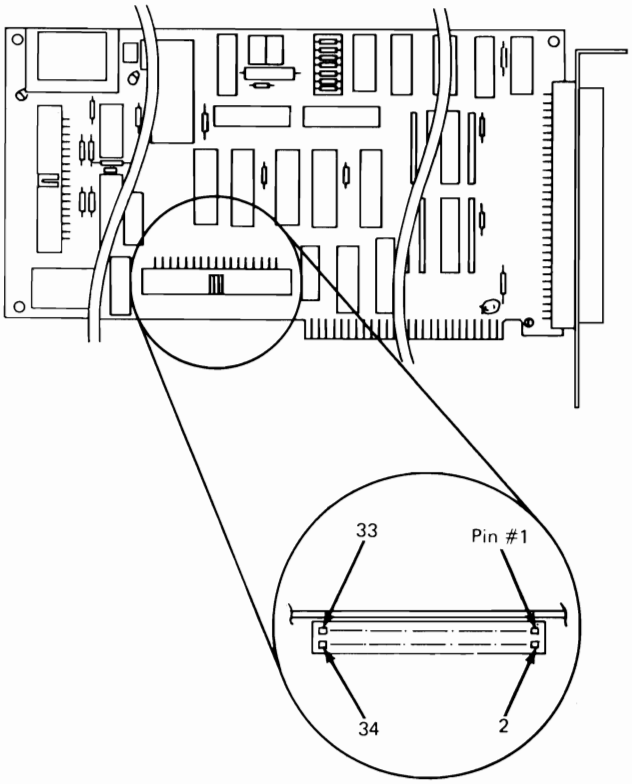


The following shows the pins of the expansion bus connector, J1, and their respective signals.

	Signal Name/Description	Pin	
	BUFF 0o	1	
	Reserved	2	
	$\overline{\text{WRITEREADGATE}}$	3	
	BUFFREAD	4	
	$\overline{\text{BUFFRES}}$	5	
	$\overline{\text{BUFFREAD}}$	6	
		7	
	$\overline{\text{IRQ}}$	8	
	Reserved	9	
	Reserved	10	
	D GND	11	Data
External	D GND	12	Acquisition
Device	Reserved	13	Adapter
	Reserved	14	
	D GND	15	
	D GND	16	
	Reserved	17	
	Reserved	18	
	$\overline{\text{AS7}}$	19	
	$\overline{\text{AS6}}$	20	
	$\overline{\text{AS5}}$	21	
	$\overline{\text{AS4}}$	22	
	$\overline{\text{AS3}}$	23	
	$\overline{\text{AS2}}$	24	
	$\overline{\text{AS1}}$	25	
	$\overline{\text{AS0}}$	26	
	$\overline{\text{AS15}}$	27	
	$\overline{\text{AS14}}$	28	
	$\overline{\text{AS13}}$	29	
	$\overline{\text{AS12}}$	30	
	$\overline{\text{AS11}}$	31	
	$\overline{\text{AS10}}$	32	
	$\overline{\text{AS9}}$	33	
	$\overline{\text{AS8}}$	34	

Expansion Bus Connector J2

The following shows the location of the expansion bus connector, J2.



The following shows the pins of the expansion bus connector, J2, and their respective signals.

	Signal Name/Description	Pin	
	$\overline{\text{WD 3}}$	1	
	D GND	2	
	HA 7 D GND	3	
	HA 6 D GND	4	
	HA 5 D GND	5	
	HA 4 D GND	6	
	DV 7	7	
	DV 6	8	
	DV 5	9	
	DV 4	10	
	LD 7	11	Data
External	LD 6	12	Acquisition
Device	LD 5	13	Adapter
	LD 4	14	
	LD 3	15	
	LD 2	16	
	LD 1	17	
	LD 0	18	
	HD 7	19	
	HD 6	20	
	HD 5	21	
	HD 4	22	
	HD 3	23	
	HD 2	24	
	HD 1	25	
	HD 0	26	
	DV 3	27	
	DV 2	28	
	DV 1	29	
	DV 0	30	
	WD 3 D GND	31	
	WD 2	32	
	WD 1	33	
	WD 0	34	

Notes:

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Switch Settings

The Data Acquisition Adapter has five groups of slide-type DIP switches that control analog output range, analog input range, adapter number, and interrupt level. Each group of switches is labeled on the adapter, and each switch is numbered on the housing. The switch positions (On and Off) also are labeled on the housing.

Analog Output Range

Following is a description of the switch blocks that control the Data Acquisition Adapter's analog output range for channels 0 and 1.

Channel 0

Switch block S1 has two switches: S1-1 and S1-2. These switches determine the relationship between analog output values and the voltage output of the analog output device.

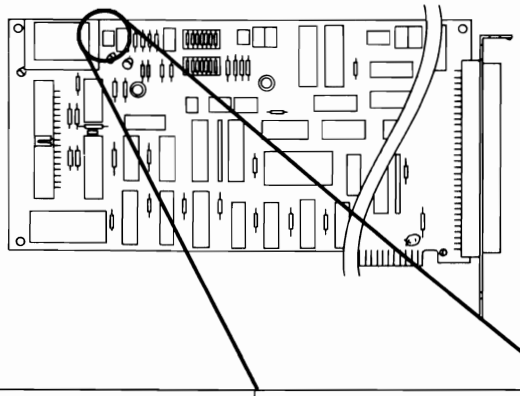
S1-1 controls voltage range:

- On: 10-volt range
- Off: 20-volt range

S1-2 controls voltage polarity:

- On: Bipolar (±) voltage
- Off: Unipolar (+) voltage

The following diagram shows the location and switch settings for switch block S1.



Input Range	Switch Settings
-5 to +5 volts	
-10 to +10 volts	
0 to +10 volts	

Note: Only the settings shown may be used for this switch block.

Channel 1

Switch block S2 has two switches: S2-1 and S2-2. These switches determine the relationship between analog output values and the voltage output of the analog output device.

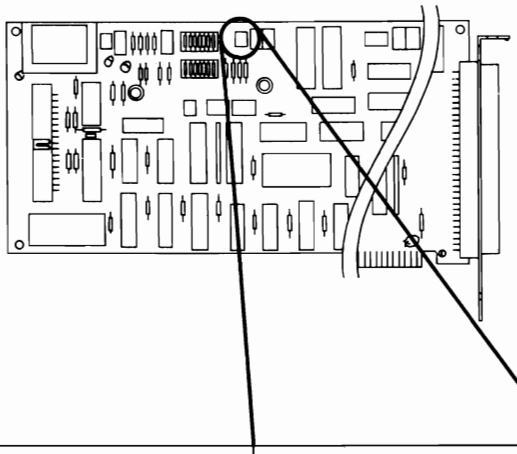
S2-1 controls voltage range:

- On: 10-volt range
- Off: 20-volt range

S2-2 controls voltage polarity:

- On: Bipolar (±) voltage
- Off: Unipolar (+) voltage

The following diagram shows the location and switch settings for switch block S2.



Output Range	Switch Settings
-5 to +5 volts	
-10 to +10 volts	
0 to +10 volts	

Note: Only the settings shown may be used for this switch block.

Analog Input Range

Switch block S3 has four switches: S3-1, S3-2, S3-3, and S3-4. The settings of these switches determine the relationship of analog input voltage to the values returned by the analog input device.

S3-1 is not used and is placed in the Off position.

S3-2 controls the 20-volt input range:

- On: 20-volt range active
- Off: 20-volt range inactive

S3-3 controls the 10-volt input range.

- On: 10-volt range active
- Off: 10-volt range inactive

S3-4 controls voltage polarity.

- On: Bipolar (±) voltage
- Off: Unipolar (+) voltage

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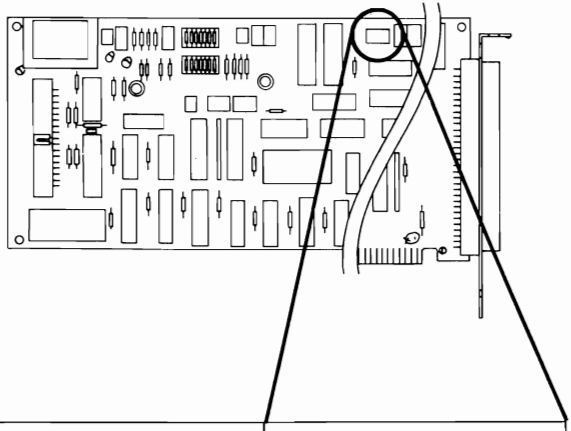
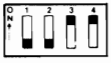
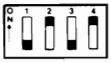
The following diagram shows the location and switch settings for switch block S3.



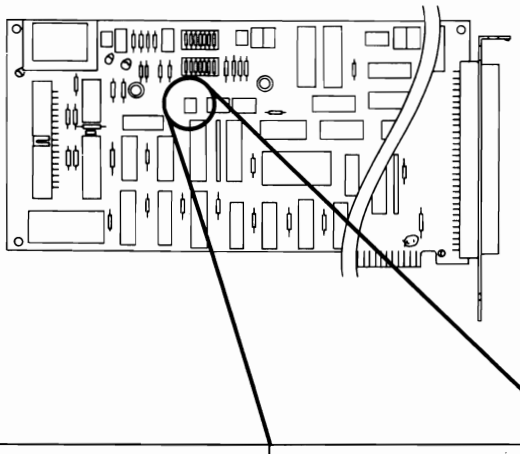
Output Range	Switch Settings
-5 to +5 volts	
-10 to +10 volts	
0 to +10 volts	

Note: Only the settings shown may be used for this switch block.

Adapter Number

Switch block S4 has two switches: S4-1 and S4-2. These switches specify the adapter number (0 through 3). Assign a number to each Data Acquisition Adapter before installation.

Note: Up to four Data Acquisition Adapters may be installed in your unit. Each adapter must be given a different adapter number.



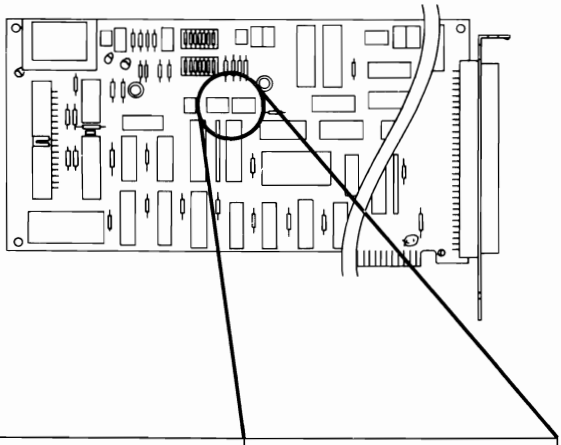
Adapter Number	Switch Positions
0	
1	
2	
3	

Interrupt Level

Switch block S5 has two 5-switch switch blocks rather than one 10-switch switch block. The switches of the right-hand, 5-switch, switch block, although numbered 1 through 5, are functionally identical to switches 6 through 10.

These 10 switches determine the interrupt level of each Data Acquisition Adapter. Set the interrupt level for each adapter before installation. Data Acquisition Adapters installed in the same unit must be set to the same interrupt level. The setting for interrupt request level 7 (IRQ7) is recommended.

The following diagram shows the location and switch settings for switch block S5.



IRQ Level	Switch Settings
7 (Recommended)	
6	
5	
4	
3	

Note: Only the settings shown may be used for this switch block.

Specifications

The following is a description of the Data Acquisition Adapter specifications and device characteristics.

Data Acquisition Adapter

Following is a description of the Data Acquisition Adapter specifications.

Dimensions

Height	99.1 mm (3.9 in.)
Height at Tab Pins	106.7 mm (4.2 in.)
Length	335.3 mm (13.2 in.)
Thickness	14.2 mm (0.56 in.)
Weight	270 g (9.5 oz)

Power Requirements

+5 volts ±5% at approximately 1 ampere typical (1.5 ampere maximum)

System Reference Voltage

Output Voltage	+10 volts
Accuracy	±1.2%
Output Load Current	±2 milliamperes maximum
Output Load Capacitance	0.5 microfarads maximum for stability
Output Protection	Protected for short to common
Output Impedance	2-ohms maximum at distribution panel connector

Environment

The Data Acquisition Adapter complies with the limits for a Class B computing device according to Subpart J of Part 13 of FCC rules and meets German VED requirements when installed in the host system.

Operating Environment

Temperature Range	+5 to +46°C (+41 to +114.8°F)
Humidity Range	8% to 80% non-condensing
Altitude	2187 m (7000 ft) maximum

Non-Operating Environment

Temperature Range	-4 to +60°C (-40 to +140°F)
Humidity Range	5% to 100% non-condensing

Data Acquisition Adapter Devices

Following is a description of the characteristics of the devices on the Data Acquisition Adapter.

Analog Output Device

The analog output device has the following characteristics:

Resolution	12 bits
Output Channels	2
Output Ranges	Switch-selectable ranges: 0 to +10 volts (unipolar), -5 to +5 volts (bipolar), and -10 to +10 volts (bipolar).
Output Load Current	±5 milliamperes minimum
Output Load Capacitance for Stability	0.5 microfarads maximum
Digital Coding	Unipolar: binary. Bipolar: offset binary.
Integral Linearity Error	± 1 least significant bit (LSB) maximum
Impedance	2-ohms maximum at the distribution panel connector
Protection	Protected for short to common

Differential Linearity Error	±1/2 LSB maximum; guaranteed monotonic
Gain Error	±0.1% maximum between ranges. Any range adjustable to zero.
Gain Stability	±35 ppm/°C of full scale range (FSR) maximum
Unipolar Offset Error	±3.25 millivolts maximum
Unipolar Offset Stability	±8ppm/°C of FSR maximum
Bipolar Offset Error	Adjustable to zero
Bipolar Offset Stability	±24 ppm/°C of FSR maximum
Power Supply Rejection	±1/2 LSB maximum change in full scale calibration
Throughput from Memory	25,000 conversions per second, minimum

Dynamic characteristics for a -10 volt to +10 volt step with less than ±5 milliamperes and less than 1000 picofarads load are:

Overshoot	±1% of FSR maximum
Settling Time	10 microseconds maximum to within ±0.1% FSR

Analog Input Device

The analog input device has the following characteristics:

Resolution	12 bits
Input Channels	4 differential
Input Ranges	Switch-selectable ranges: 0 to +10 volts (unipolar), -5 to +5 volts (bipolar), and -10 to +10 volts (bipolar).
Input Resistance	100 megohms minimum
Input Capacitance	200 picofarads maximum; measured at the distribution panel connector
Input Leakage Current	±300 nanoamperes maximum
Input Current	±4 milliamperes at maximum input voltage
Digital Coding	Unipolar: binary. Bipolar: offset binary.
Safe Input Voltage	±30 volts maximum (power On or Off)
Power Supply Rejection	±1/2 LSB maximum change full scale calibration
Integral Linearity Error	±1 LSB maximum

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Differential Linearity Error	±1/2 LSB maximum
Differential Linearity Stability	±5 ppm/°C maximum; guaranteed monotonic
Gain Error	±0.1% maximum between ranges. Any range adjustable to zero.
Gain Stability	±32 ppm/°C of FSR maximum
Common-Mode Input Range	±11 volts maximum
Common-Mode Rejection	72 dB minimum ratio (signal within common-mode range)
Unipolar Offset Error	Adjustable to zero
Unipolar Offset Stability	±24 ppm/°C of FSR maximum
Bipolar Offset Error	Adjustable to zero
Bipolar Offset Stability	±24 ppm/°C of FSR maximum

Settling Time	For channel acquisition: 20 microseconds maximum to ±0.1% of the input value
Conversion Time	35 microseconds maximum
Throughput to Memory	15,000 conversions per second, minimum
'A/D convert enable'	
Input Impedance	One LS TTL load plus 10-kilohm pull-up resistor
'A/D convert out'	
Fanout	10 LS TTL loads or 2 standard TTL loads

Binary Device

The binary device has the following characteristics:

Binary Input (BI0 through BI15)

Input Impedance	One LS TTL load plus 10-kilohm pull-up resistor
Throughput to memory	25,000 operations per second, minimum

$\overline{\text{BI HOLD}}$

Input Impedance	Two LS TTL loads plus one 10-kilohm pull-up resistor

'BI Strobe'

Input Impedance	One LS TTL load plus one 10-kilohm pull-up resistor

BI CTS

Fanout	10 LS TTL loads or 2 standard TTL loads

Binary Output (BO0 through BO15)

Fanout	28 LS TTL loads or 7 standard TTL loads
Throughput from Memory	25,000 operations per second, minimum
'BO Gate'	
Input Impedance	Two LS TTL loads plus one 10-kilohm pull-up resistor
BO CTS	
Input Impedance	One LS TTL load plus 10-kilohm pull-up resistor
'BO Strobe'	
Fanout	10 LS TTL loads or 2 standard TTL loads

32-Bit Timer Device

The 32-bit timer device has the following characteristics:

Counter 0

CLK 0 Frequency 1.023 MHz

'Rate Out'

Fanout 10 LS TTL loads or 2 standard TTL loads

Counter 1

'Delay Out'

Fanout 10 LS TTL loads or 2 standard TTL loads

16-Bit Timer/Counter Device

The 16-bit timer/counter device has the following characteristics:

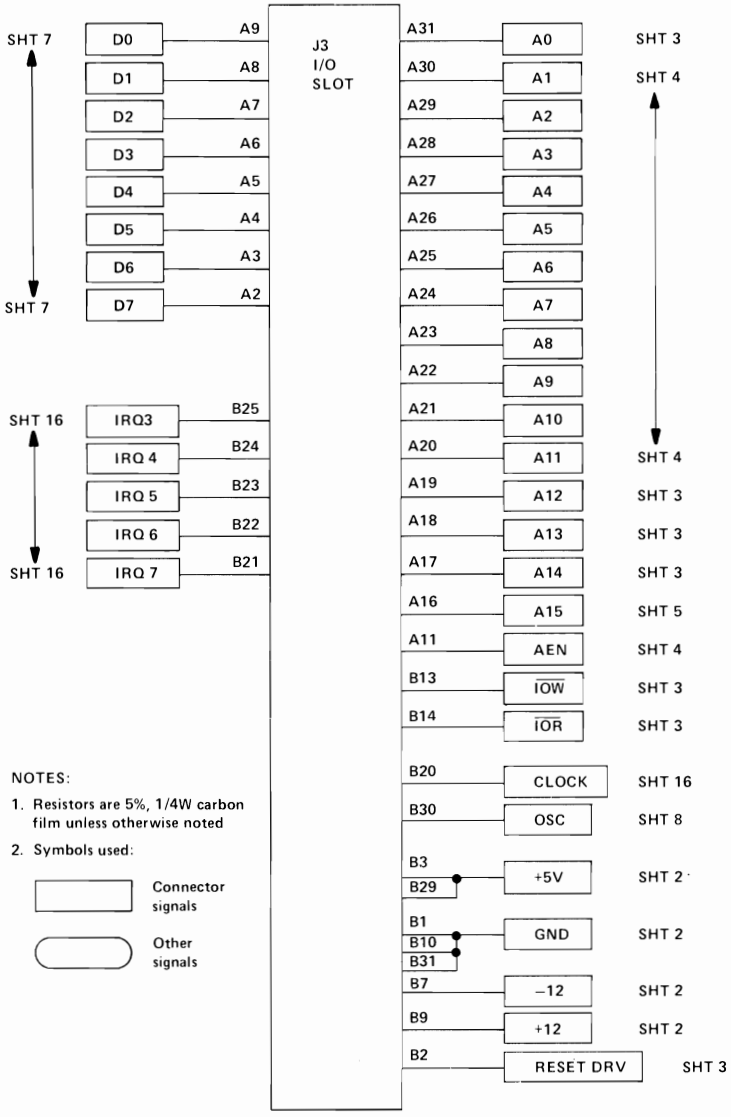
'Count In'

Input Impedance	One LS TTL load plus 10-kilohm pull-up resistor
Input Frequency	DC - 2 MHz (50% duty cycle)

'Count Out'

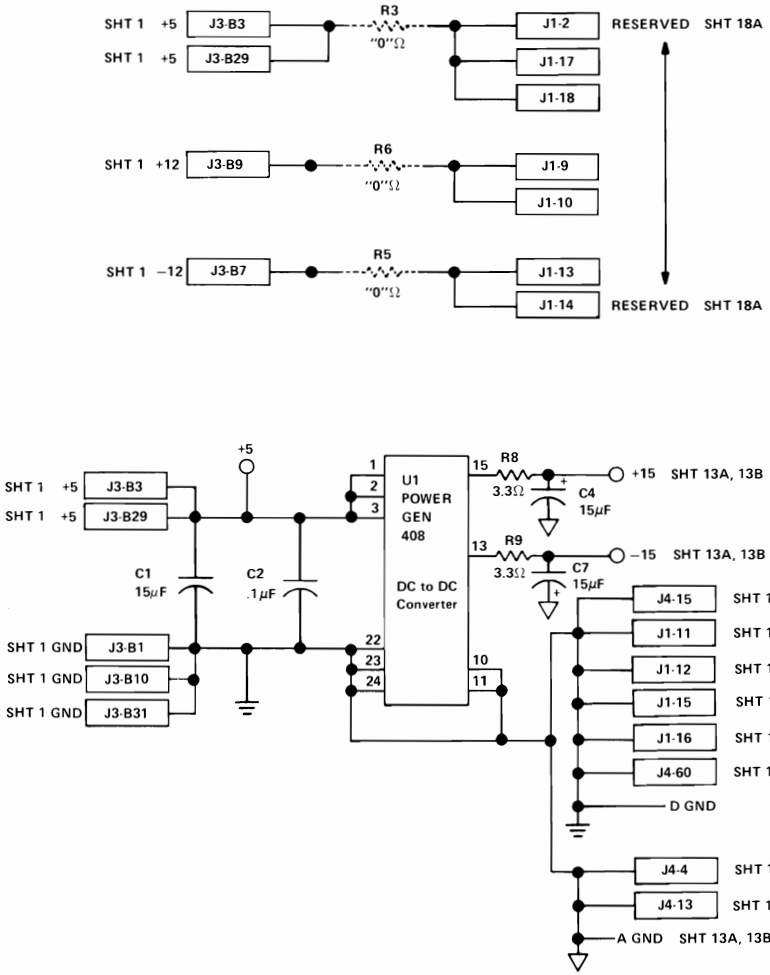
Fanout	10 LS TTL loads or 2 standard TTL loads

Logic Diagrams

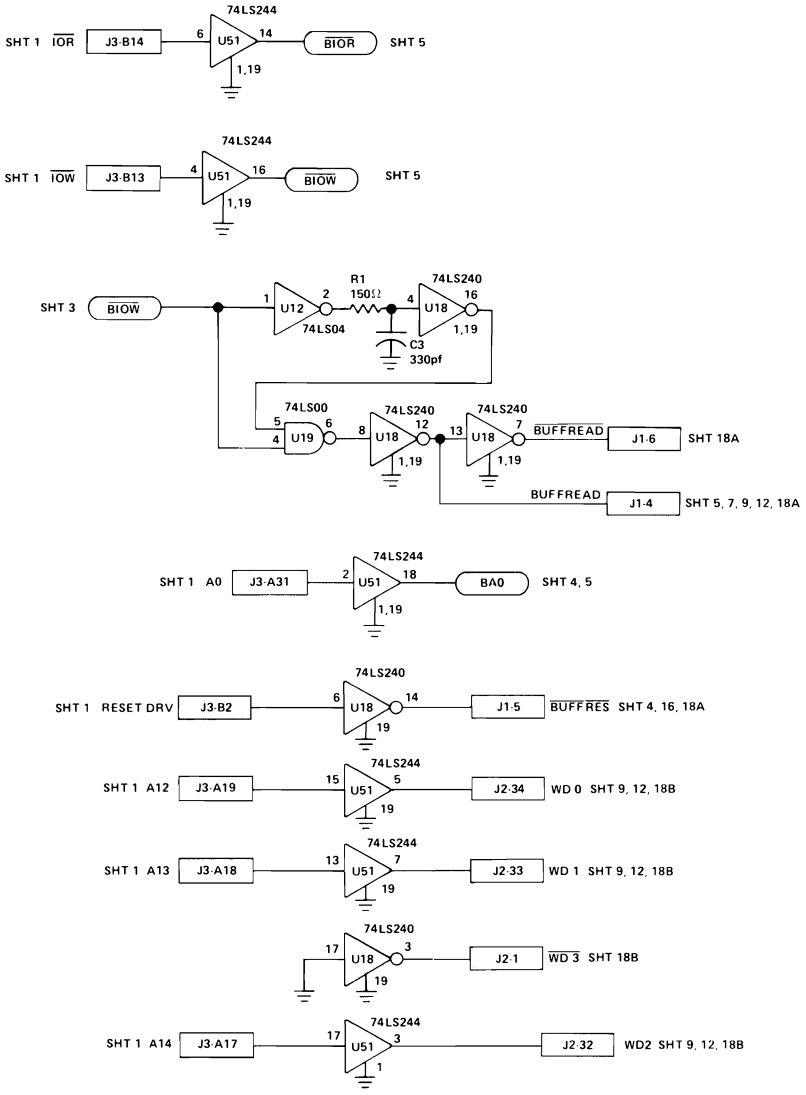


I/O Slot J3 **Sheet 1**

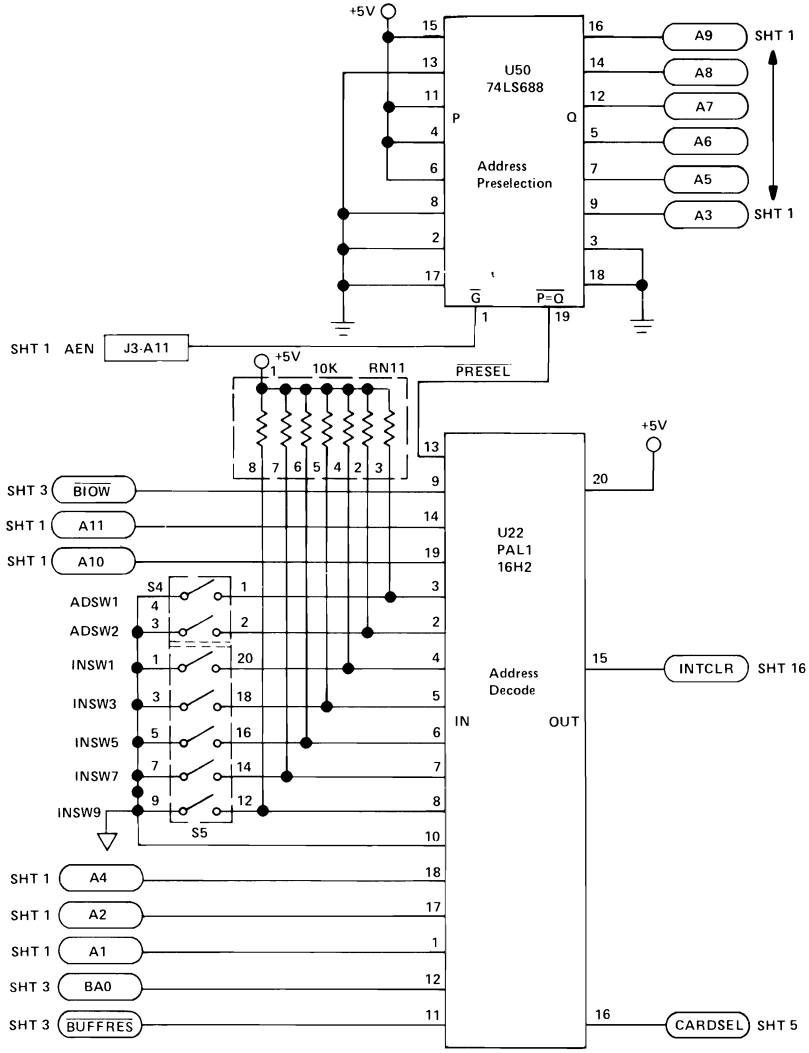
NOTE: R3, R5, R6 ARE NOT INSTALLED.



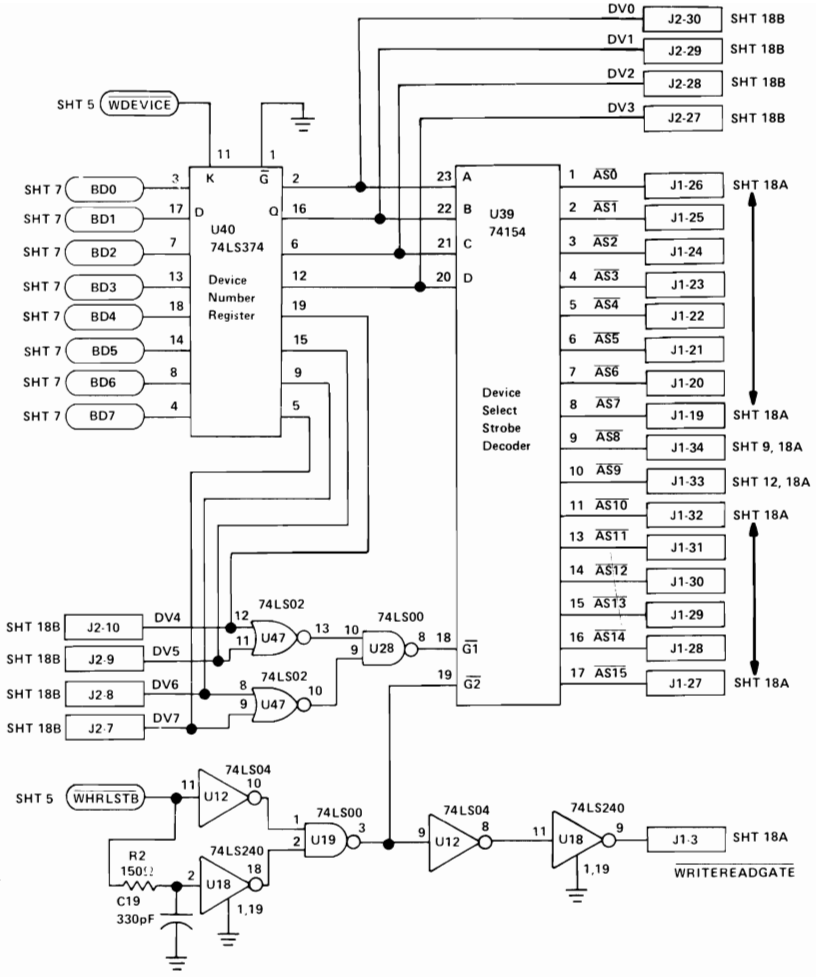
Power Supplies and Grounds **Sheet 2**



System Bus Control and Address Lines **Sheet 3**



Address Decode **Sheet 4**



Device Selection **Sheet 6**

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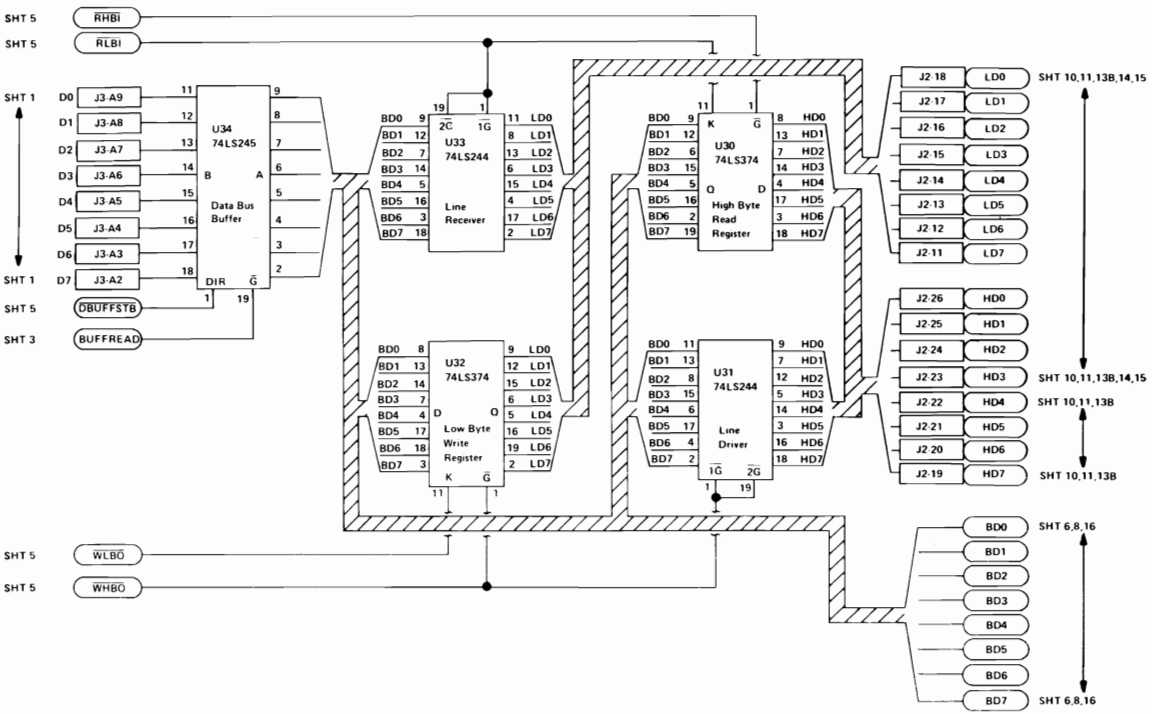

Data Bus Conversion **Sheet 7**

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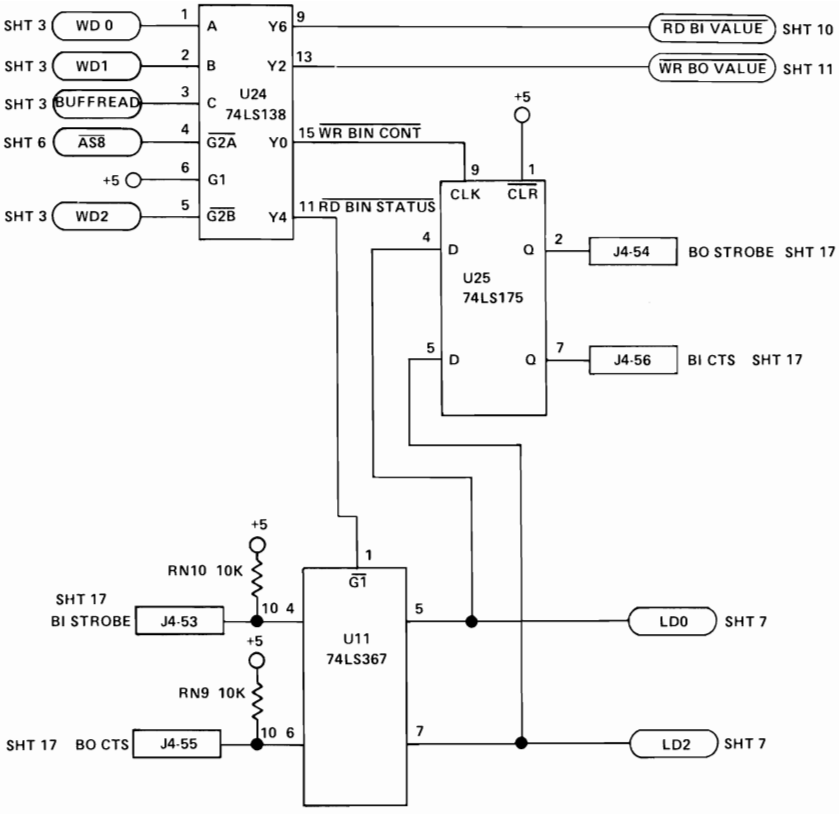
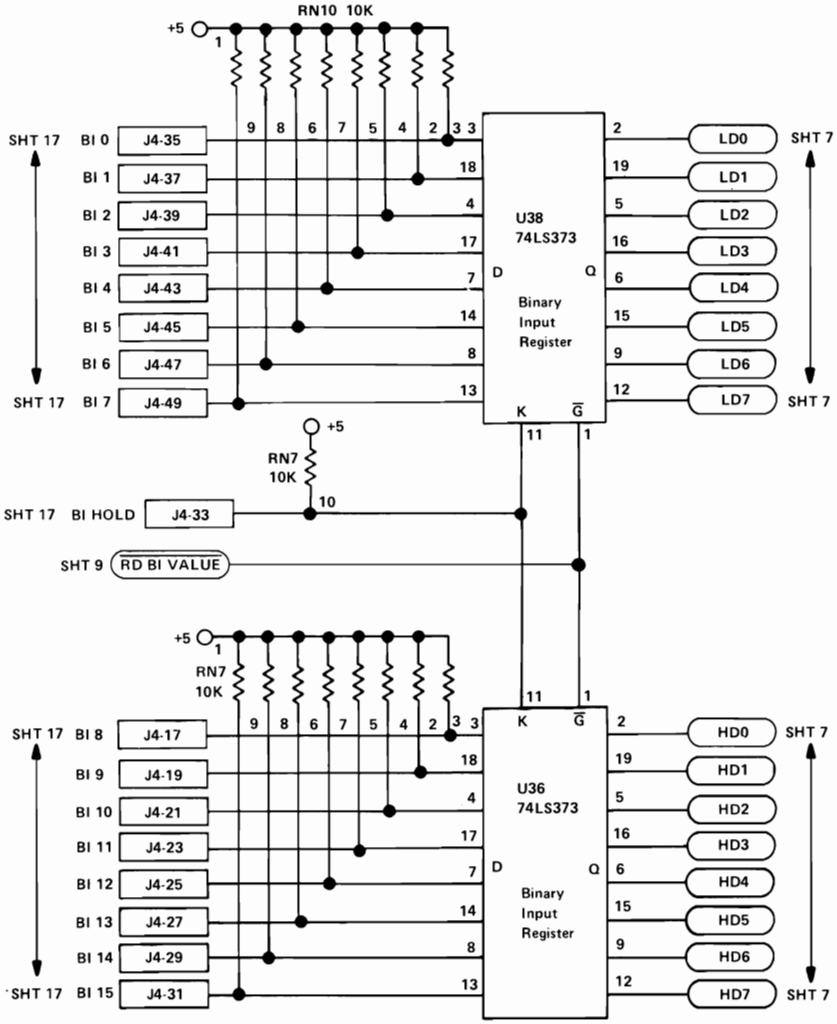
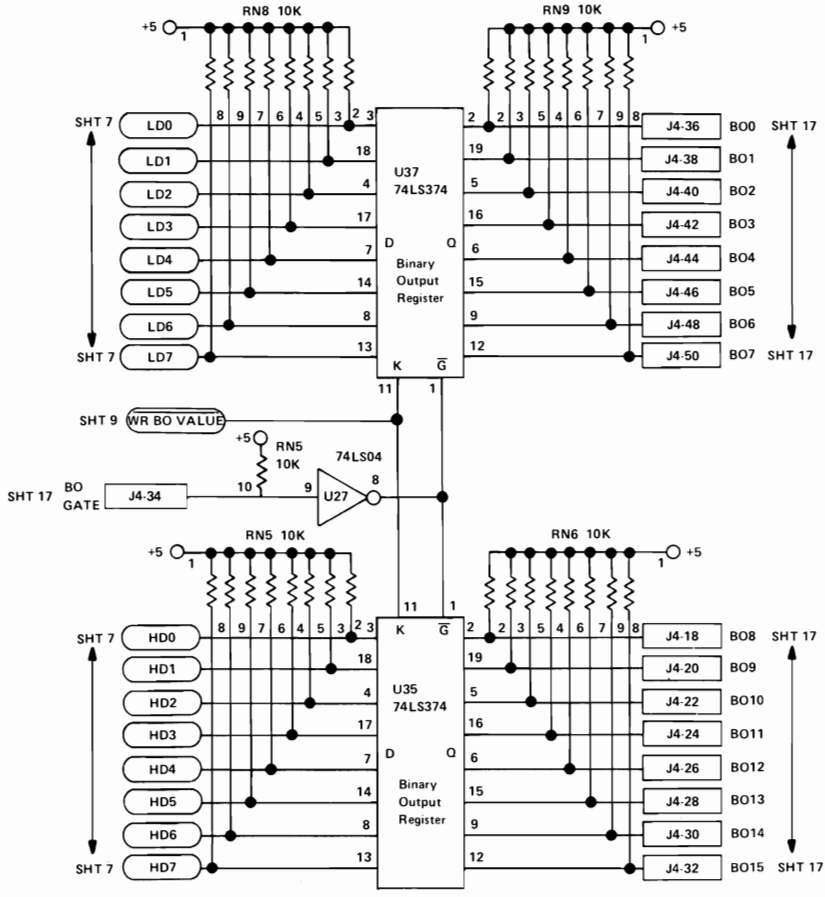


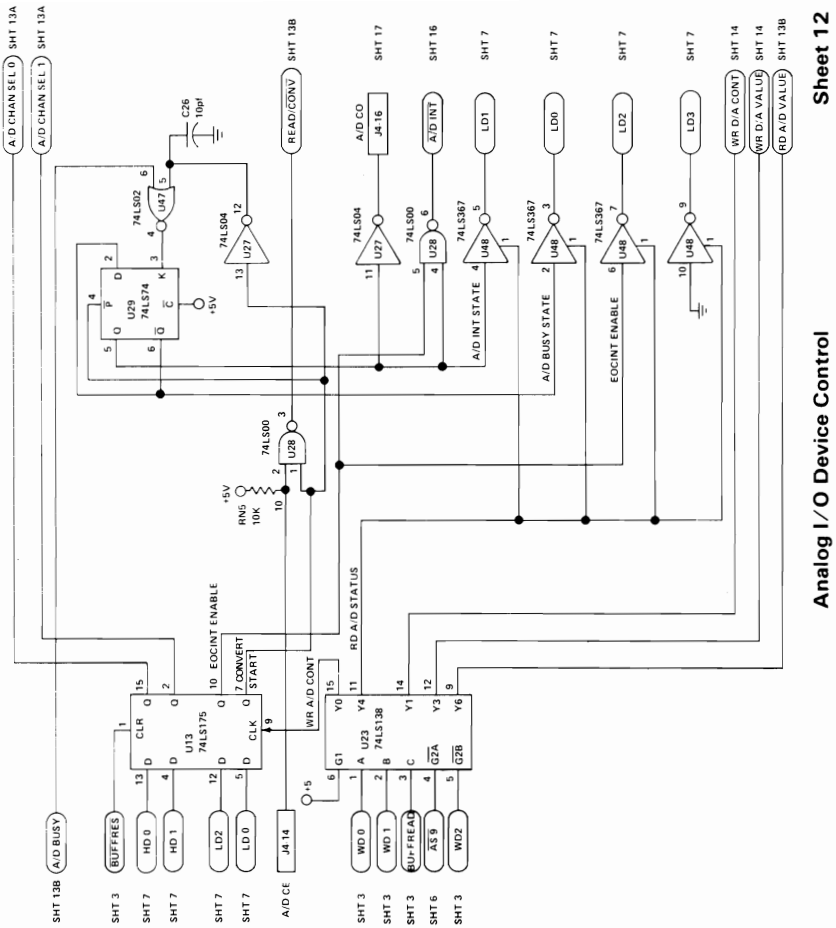
Binary I/O Device Control Decode **Sheet 9**

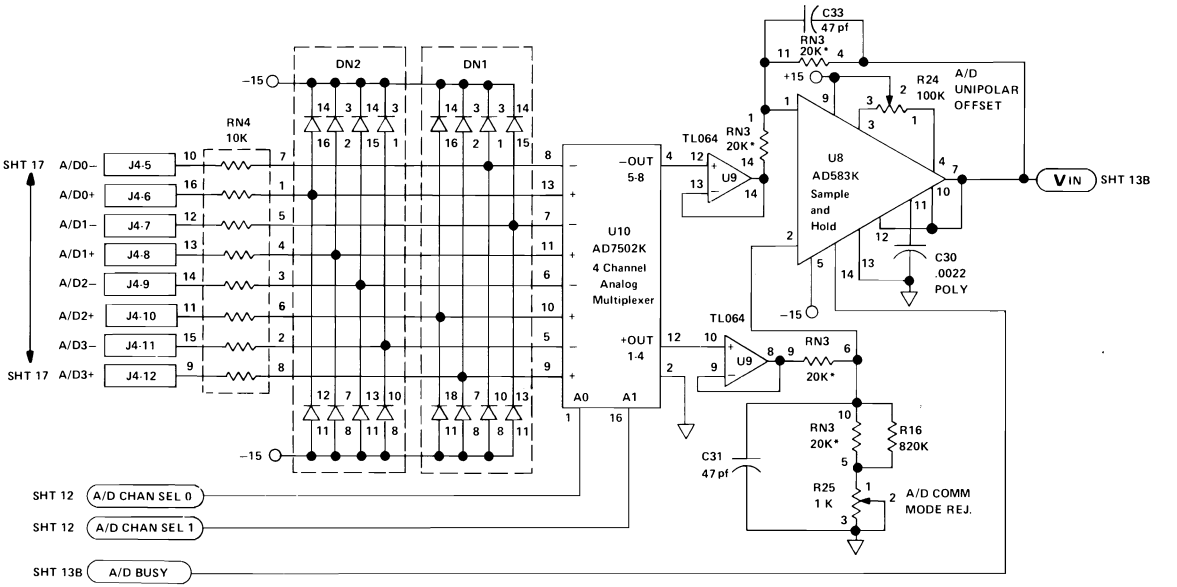


Binary Input Device **Sheet 10**



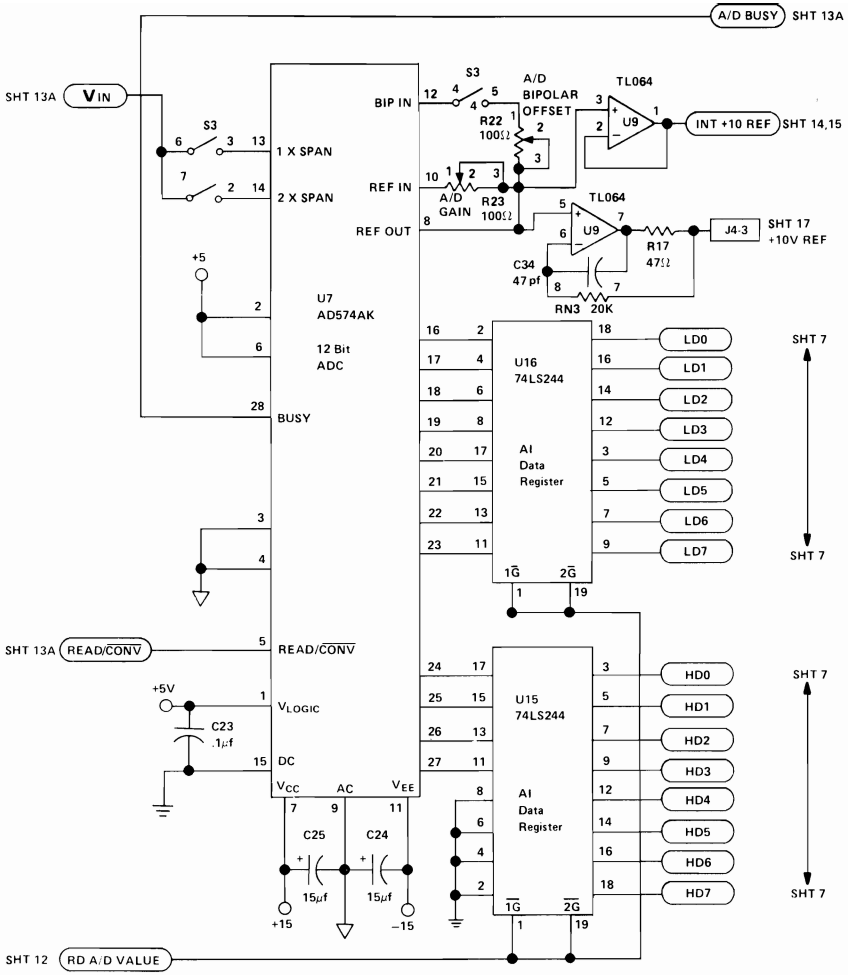
Binary Output Device **Sheet 11**



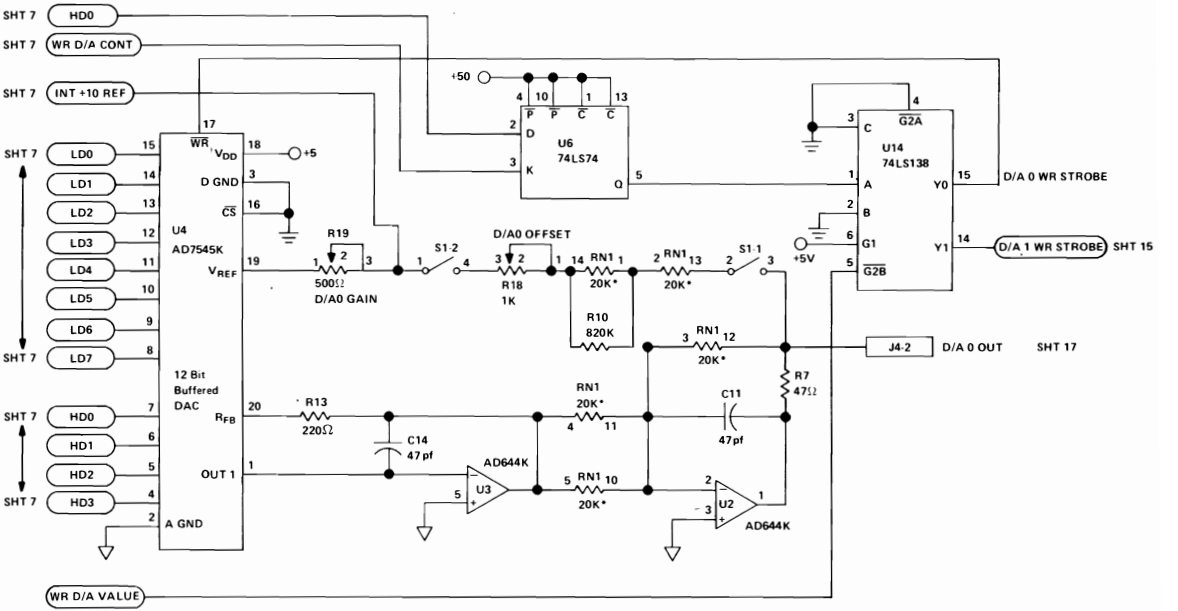


Analog Input Device Channel Multiplexer and Sample and Hold

Sheet 13A

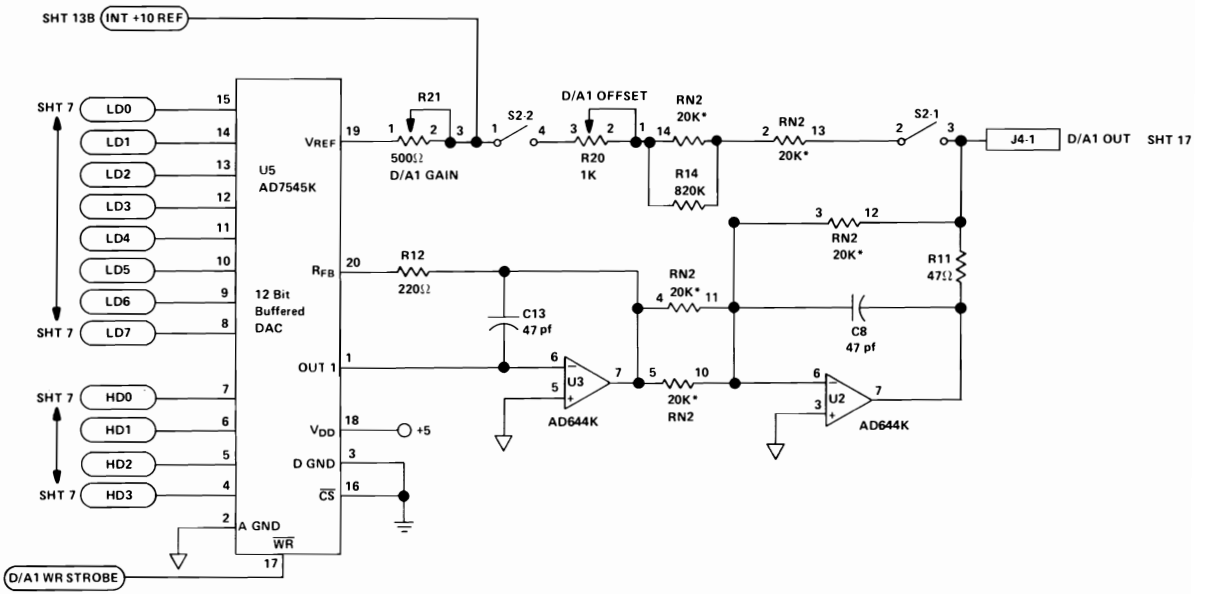


Analog Input Device
ADC AI Data Register **Sheet 13B**



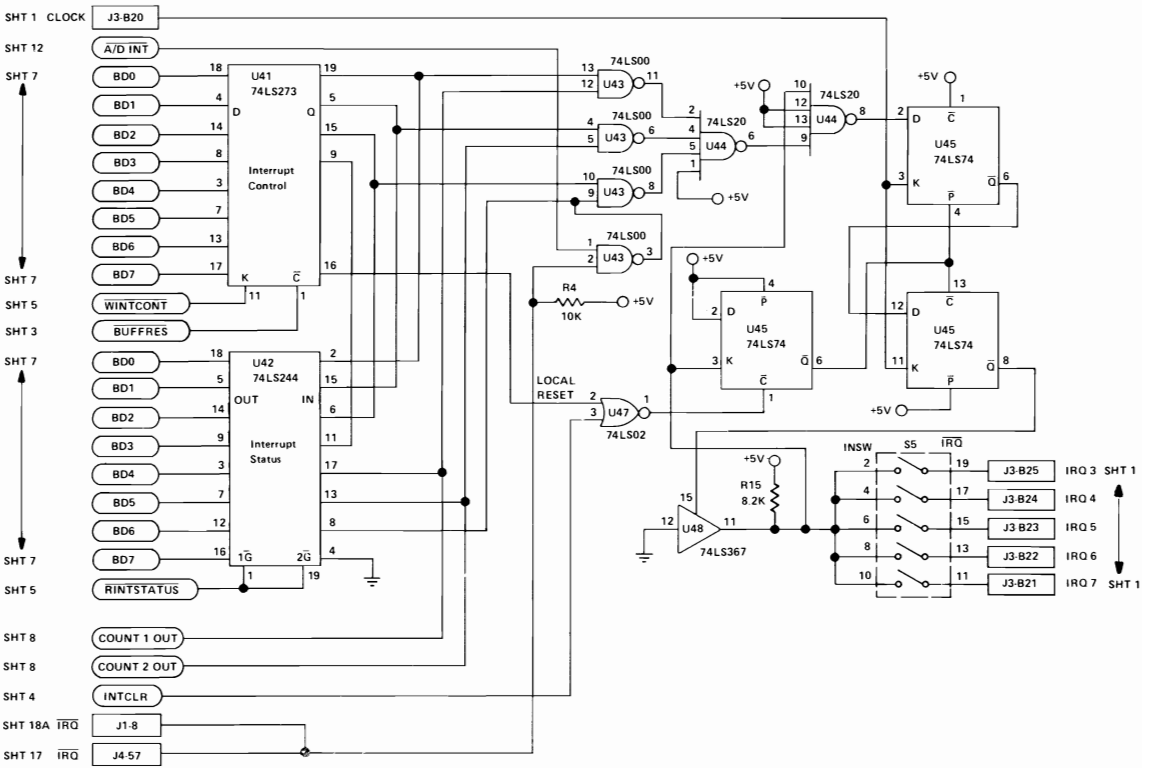
Analog Output Device
DAC for Channel 0

Sheet 14

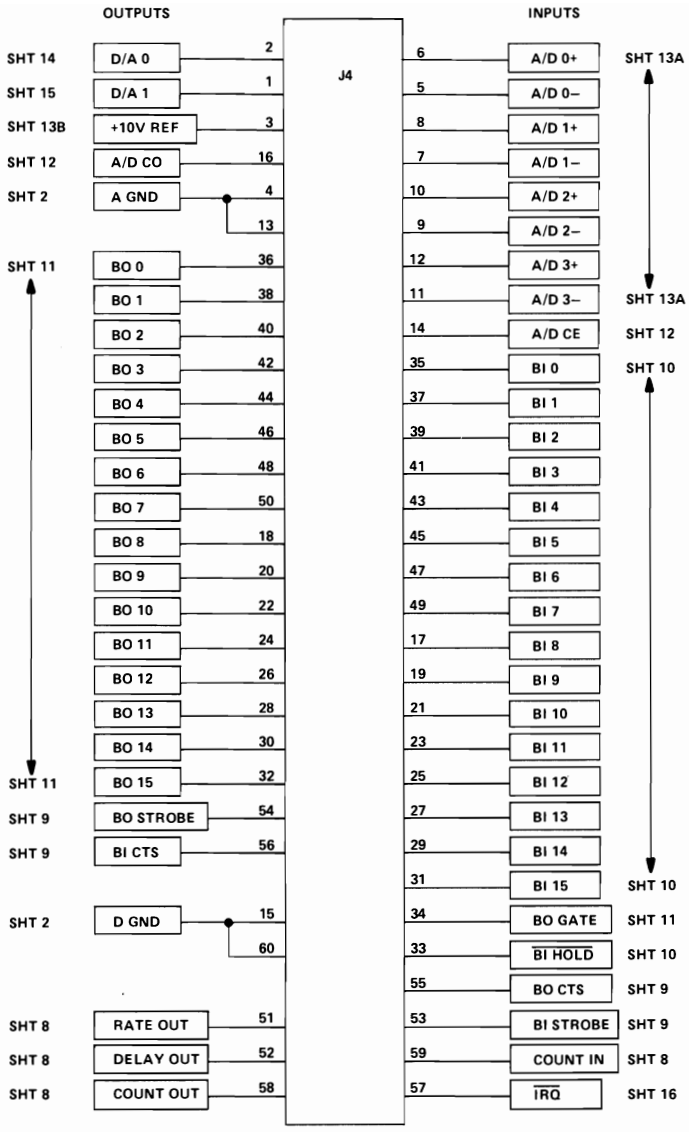


Analog Output Device
DAC for Channel 1

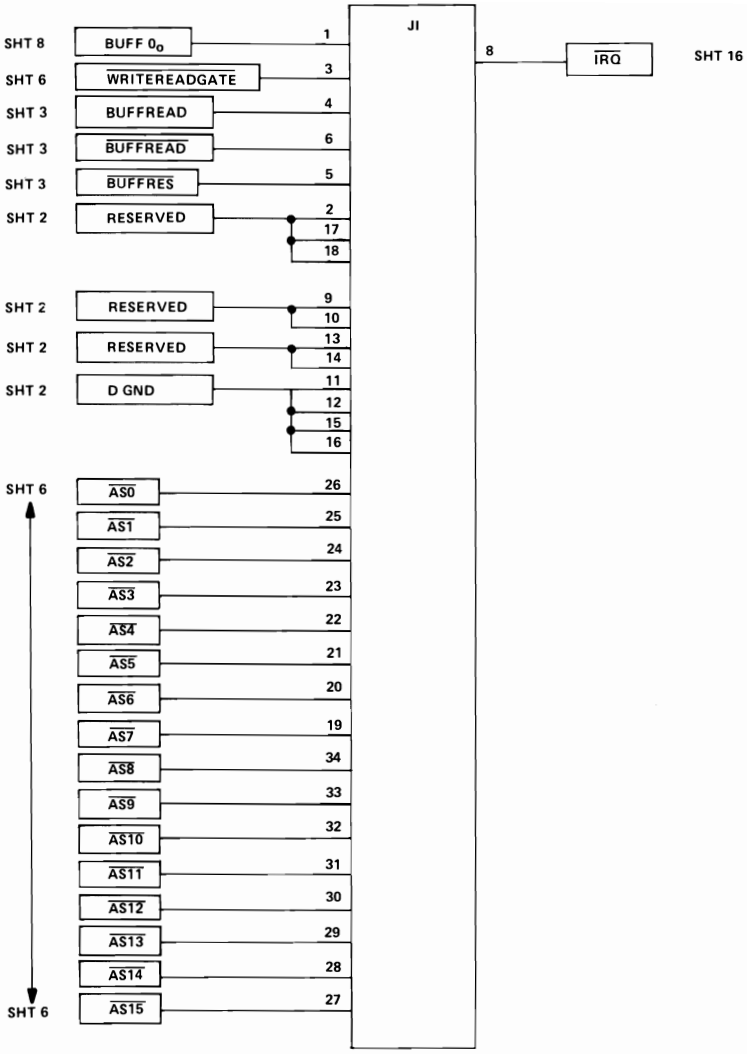
Sheet 15



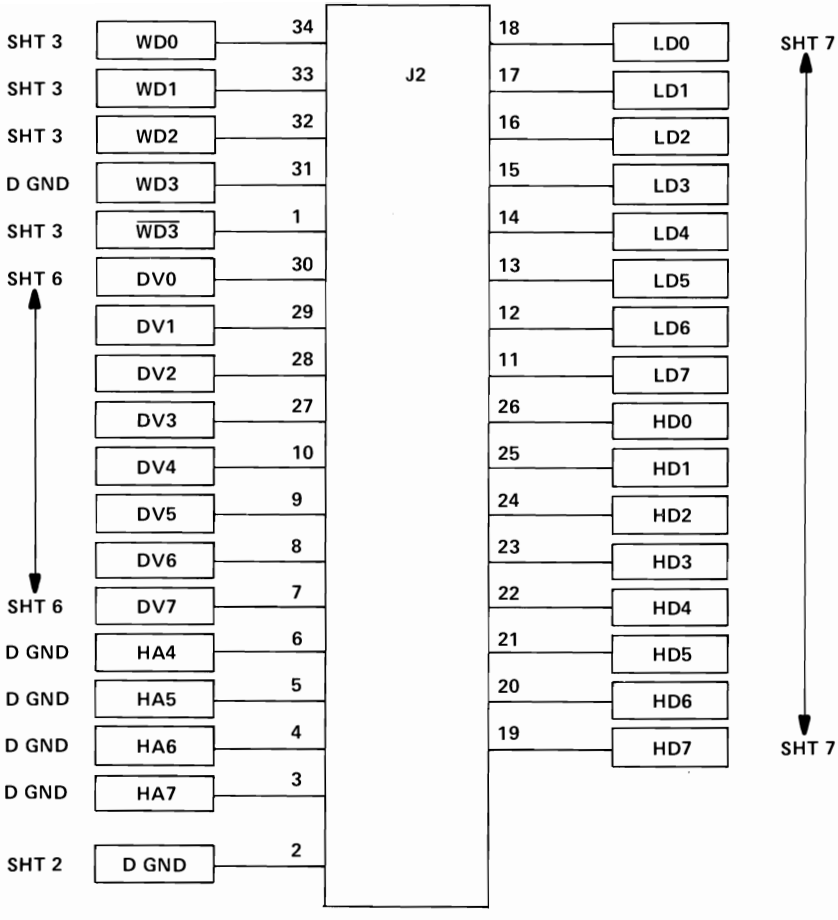
Interrupt Status and Control **Sheet 16**



Distribution Panel Connector J4 **Sheet 17**



Expansion Bus Connector J1 **Sheet 18A**



Expansion Bus Connector J2 **Sheet 18B**

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